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Compensation Techniques for Internal CMOS Operational Amplifiers

BY

Guy Fortier

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE

OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

SPRING 1987

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled Compensation Techniques for Internal CMOS Operational Amplifiers submitted by Guy Fortier in partial fulfilment of the requirements for the degree of Master of Science.

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(Supervisor)

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Date: January 30, 1987

ABSTRACT

A novel compensation technique for internal two-stage CMOS op amps is presented. Instead of connecting the compensation capacitor across the output stage for the Miller multiplication effect, a separate matched 'compensation' stage is used. The RHP zero is eliminated and the nondominant pole becomes independent of the load capacitance resulting in a 20^{o} improvement in the phase margin for the same power dissipation. The achievable performance for this type of compensation in areas such as power dissipation, settling time, phase margin, die area, and power supply rejection is compared with the other compensation schemes found in the literature. Designs based on a common set of specifications were generated using the different compensation techniques. The step response of the unity gain configuration was studied using SPICE simulations. The simple capacitor compensation and the separate stage compensation designs were integrated. The measurements for a sample of 5 chips are given. General design of internal two-stage CMOS op amps is discussed and a systematic design method is presented.

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LIST OF SYMBOLS

A_1	differential input voltage gain (open loop) at doublet frequency
Acm	common mode input voltage gain
Av(0)	differential input voltage gain (open loop) at DC
Av, A_{OL}	differential input voltage gain (open loop)
Av_{DD}, Av_{SS}	voltage gain from power supplies to output
Cc	compensation capacitor
C_L	load capacitor
CMRR	common mode rejection ratio
Cox	gate oxide capacitance
C_p	parasitic capacitance
f_u	op amp unity gain frequency
f_T	transistor unity current gain frequency
GBW	gain-bandwidth product
g_m	transistor transconductance
g_{mb}	transistor transconductance from substrate
I_1	op amp first stage bias current
I_2	op amp second stage bias current
ICMR	input common mode range
I_{M6}	second stage driver current
I_{tot}	op amp total bias current
k	ratio of doublet pole and zero
k_B	Boltzmann's constant 1.38×10^{-23} J/K
K	factor describing ratio of transconductances of first stage input pair and mirror load transistors

K'	= μCox (intrinsic transconductance parameter)
KF	flicker noise coefficient
L	transistor device length
Mp	peak percentage overshoot in step response
OA	operational amplifier
OS	output swing
p	Laplace transfer function pole frequency
p'	= p/w_u (normalized pole location)
P_{diss}	power dissipation
PM	phase margin
PSRR	power supply rejection ratio
Ro	buffer output resistance
SPICE	analog circuit simulation software package
SR	slew rate
t_S	step response settling time
Vcm	DC common mode input voltage
v_{cm}	small signal AC component of common mode input voltage
Vdmm	DC voltage measured on digital multimeter
V_{DS}	transistor drain-source voltage
V_{DSAT}	transistor drain-source saturation voltage
V_{GS}	transistor gate-source voltage
Vi,Vo	input and output voltages
v_i, v_o, vo	small signal AC component of input and output voltages
v_n	rms noise voltage
$\overline{v_N^2}$	mean of normalized noise power

Vos	offset voltage
Vo^+, Vo^-	positive and negative output voltages
V_S	voltage stepsize
V_{SB}	transistor source-body voltage
V_{SS}, V_{DD}	DC power supply voltages
vss, vdd	AC small signal component of power supply voltages
V_t	transistor threshold voltage
V_{to}	transistor threshold voltage with $V_{SB} = 0$
w_u	op amp unity gain frequency (radians/sec)
w_z	doublet zero frequency (radians/sec)
W	transistor device width
X_d	width of depletion region between transistor channel pinch-off point and drain
β	$= \mu Cox(W/L)$ (transconductance parameter)
ϵ	step response error band factor
γ	body effect parameter [1]
λ	transistor output resistance parameter [1]
μ	electron (hole) mobility
ϕ_F	Fermi level [1]
τ_u	$= 1/w_u$ (time constant)
τ_z	$= 1/w_z$ (time constant)

1.0 INTRODUCTION

1.1 Applications of op amps

Since their introduction in the mid-60's, monolithic operational amplifiers (or 'op amps') have become the most widely used type of analog integrated circuit [16]. The op amp is a general purpose amplifying device which is used in a closed feedback loop. The op amp together with its external feedback components forms an 'operational circuit' [12]. Part of the appeal of the op amp lies in the fact that ideally, its characteristics are such that the input-output relationship for the operational circuit becomes solely dependent on the external feedback components. Hence the transfer function becomes insensitive to integrated circuit process tolerances which result in variation of the op amp parameters. This desirable behaviour is most closely achieved as the op amp approaches the ideal of having infinite gain and bandwidth, infinite input resistance and zero output resistance. By only varying the external feedback components then, the operational circuit can be made to perform various analog signal processing functions such as precision gain, inversion, addition, subtraction, integration, differentiation and even nonlinear operations such as exponentiation. This, together with its low cost and small size due to integration, have brought the op amp into use in countless applications [17].

1.2 CMOS realization of op amps

Because of the economic advantages of implementing both digital and analog functions on the same chip, it is desirable to realize op amps in CMOS. CMOS is the technology of choice for digital circuits, resulting in lower power dissipation and higher circuit densities compared to both NMOS and bipolar implementations [20]. Analog functions requiring op amps are often needed for interfacing digital systems to the outside world. Some of these functions include filtering, voltage comparison, generation of reference voltages and the sample and hold function. Improvements in process technology now allow these analog functions to be implemented on the same chip as the digital circuitry resulting in more cost effective products [13]. Examples of subsystems in which this has occurred are A/D converters, digital signal processors and PCM voice encoders.

Using CMOS for analog circuits instead of the traditional bipolar implementation shows both advantages and disadvantages. The disadvantages are the lack of a floating diode structure, higher low-frequency noise, and lower transistor transconductance by typically an order of magnitude for the same bias current [18]. This last fact results in order of magnitude higher DC offsets, increased temperature sensitivity and lower gain. The typical CMOS op amp gain is 5000 versus a minimum of 50,000 for the common μA741 bipolar op amp.

Some of the advantages of CMOS are its greater circuit density (op amps are 3-5x smaller in area [18]), its ability to implement a good switch and the very high input resistance of its transistors. The latter two facts allow the use of switched capacitor techniques for

reducing the high noise and offset levels of op amps [13]. Switched capacitors can also simulate large resistance values which could not normally be integrated due to area constraints. Because of this, switched capacitor filters are a common application for CMOS op amps [13].

1.3 Two categories of op amp

Because CMOS op amps are usually used within integrated systems, their loads are often well-defined and purely capacitive with a value of only a few picofarads. Hence these 'internal' op amps [1] do not require the usual additional stage which provides a low output resistance. In contrast, a stand-alone op amp [1] needs an output stage because it is required to drive variable loads with capacitance of up to several hundred picofarad and resistance as low as a few thousand ohms. Thus, the output resistance of the internal CMOS op amp is typically several hundred thousand ohms while that of a stand-alone op amp such as the μA741 is 75 ohms.

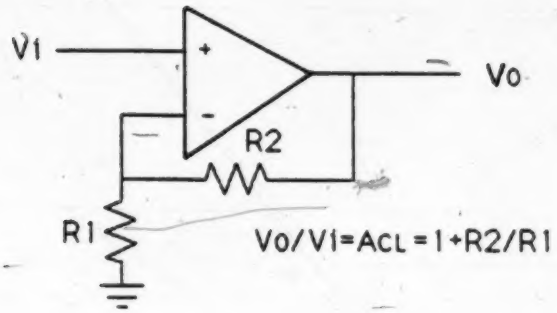
1.4 Stability and compensation of op amps

It is essential that the op amp be capable of stable operation in a closed-loop feedback configuration. In the time domain this translates into a desirable transient response such as a step response with little overshoot or ringing and fast settling. In the frequency domain stability implies a flat passband with little peaking of the frequency characteristic (assuming the most simple application as an amplifier -

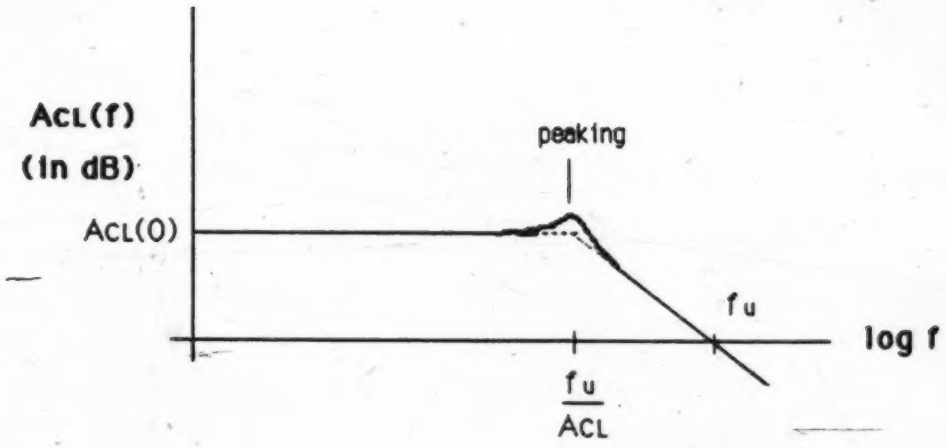
see figure 1.1) [19]. Op amp compensation aims at shaping the open-loop frequency response such that in the closed-loop feedback configuration the desired stability is achieved. Basic feedback theory [14] indicates that the total phase shift of the signal through the loop (i.e. the amplifier with its feedback circuit) must not exceed 180° for frequencies where the loop gain is still greater than unity. (Note here that the additional 180° due to inversion within the op amp is not included). A measure of the degree of stability is given by the 'phase margin' which is the amount by which the phase shift falls short of the 180° limit at the unity gain frequency. Generally, a higher phase margin results in less overshoot and ringing of the closed-loop transient response and less peaking of the frequency response.

The frequency response of the uncompensated op amp has closely spaced poles introduced by parasitics in each stage [19]. Each pole contributes a gradually increasing phase shift of up to 90° for frequencies above approximately ten times the pole frequency. The closed-loop feedback circuit with an uncompensated op amp is unstable because the op amp's closely spaced poles cause its phase shift to reach the 180° limit for greater than unity gain. The role of the compensation is to introduce a dominant pole at low frequency to roll off the gain characteristic such that the unity gain frequency occurs at a frequency lower than the next nondominant pole. A positive phase margin is then assured (see figure 1.2).

The correspondence between phase margin and closed-loop response is based on the assumption of a single nondominant pole. For this simple case the nondominant pole location determines the closed-loop frequency



(a)



(b)

Figure 1.1 Typical closed-loop frequency response for non-inverting amplifier application.

(a) circuit configuration

(b) frequency response

and transient responses and also the phase margin. Hence the phase margin itself can be used to predict the closed-loop responses. However, the actual op amp usually has additional poles and zeros at higher frequency which affect the open-loop response as shown in figure 1.2. In this case the correspondence between phase margin and closed-loop response is only an approximation. The accuracy of the approximation improves as the higher order poles and zeros are located further from the second pole (see section 3.1.2).

The most basic compensation method for internal CMOS op amps is achieved by a capacitor placed across the input and output of the second gain stage [1]. The Miller multiplication effect results in a large shunt capacitance at the first stage output which, together with the high output resistance gives the required dominant pole for compensation. This simple technique works better in bipolar implementations than in CMOS. The phase margin is degraded due to the parallel signal path to the output through the compensation capacitor and this effect is more evident in CMOS due to the lower device transconductance. Using a buffer or resistor in series with the capacitor are techniques which have appeared in the literature [4,5] for solving this problem.

1.5 Thesis content

This thesis investigates four compensation techniques used in internal CMOS op amps. The four techniques are:

1) using a single Miller capacitor;

2) using a series buffer with the capacitor;

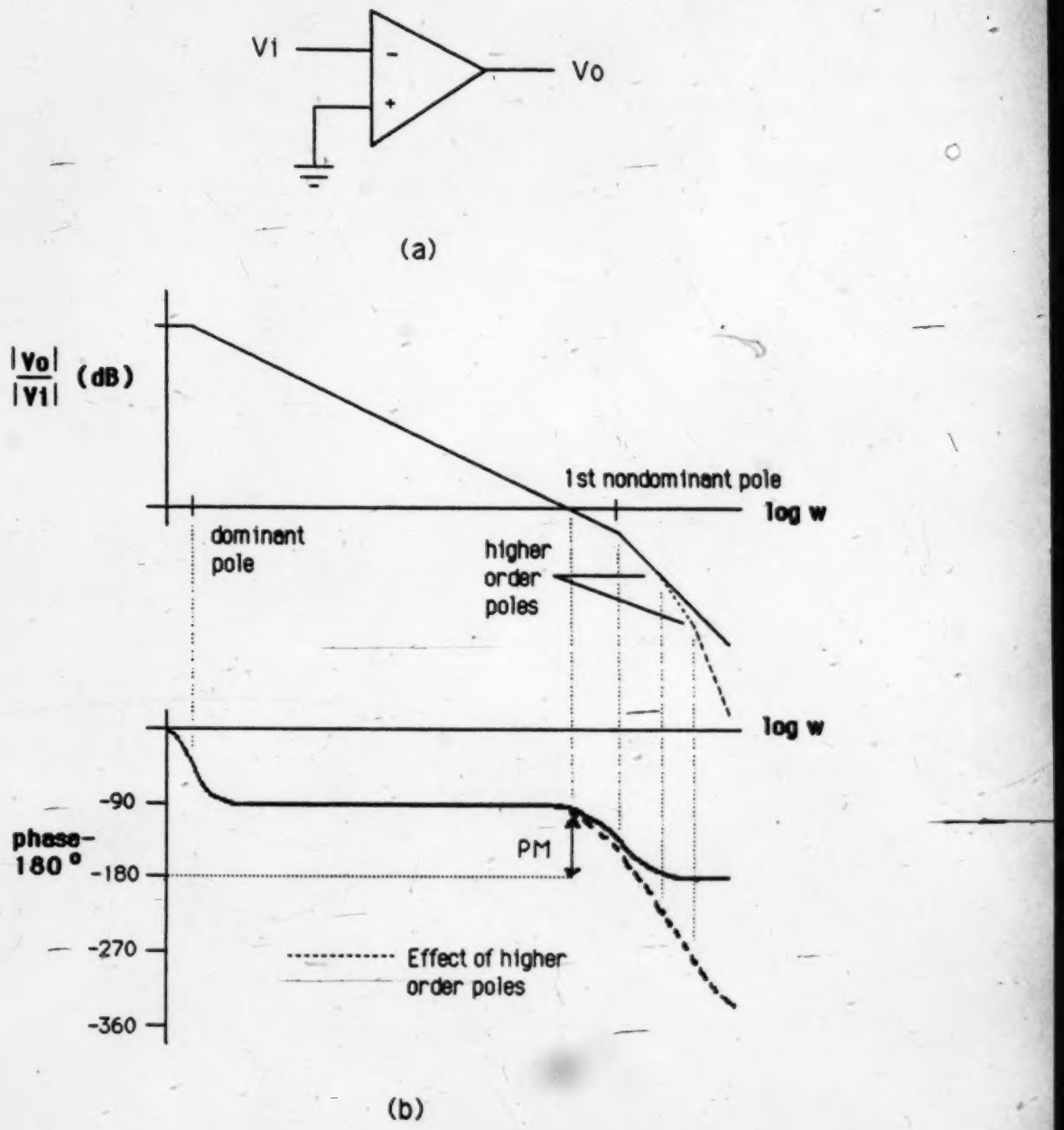


Figure 1.2 Open-loop frequency response

(a) circuit configuration

(b) magnitude and phase response

3) using a series resistor with the capacitor; and

4) using a single Miller capacitor on a separate compensation stage.

While the first three methods are widely reported in the literature, the fourth method is new to the author's knowledge. Instead of the compensation capacitor being placed across the second stage for the Miller multiplication effect, it is placed across a separate matched 'compensation' stage. Because the compensation capacitor is isolated from the output node the signal feedthrough problem is not observed. Also, as opposed to the simple capacitor compensation, the nondominant pole location becomes independent of the load capacitance. These facts result in superior compensation.

It was desired to evaluate the different compensation techniques as to their achievable performance. Partly due to the different size of compensation capacitor required and partly due to the different circuit architecture, the noise power dissipation, power supply rejection and required die area can differ for a given transient response depending on the technique which was used. The simple capacitor compensation was used as a benchmark against which the other techniques were compared. The compensation was aimed at obtaining a desirable transient response and especially a reduction of the settling time (op amp settling time is one of the factors which limits the input frequency range of switched capacitor filters). Only 100% feedback resulting in unity gain was considered because this configuration presents the most stringent compensation requirement.

Designs based on a common set of design specifications were generated using all four techniques. The results of SPICE simulations

on these designs are given. The simple capacitor compensation and the separate stage compensation designs were integrated and measurements on a sample of 5 chips are given.

One chapter is devoted to the general design of internal CMOS op amps. Seeking an optimum design can become quite a complicated matter as there are approximately twelve specifications which may have to be met and about the same number of independent circuit parameters which can be adjusted. The performance areas are often interrelated which can result in conflicting design requirements. A systematic design method is presented with the aim of providing the details of the design procedure which most texts fail to include. It is hoped that the information will be of use to other graduate students requiring the implementation of op amps in their research.

2.0 OP AMP DESIGN

2.1 Basic two-stage architecture

The design methods of this chapter are based on the two-stage architecture of figure 2.1. The first stage consists of the differential input pair M1/M2 driving the current mirror load M3/M4 with M5 providing a constant current bias. As well as giving gain, this stage provides differential to single-ended conversion with good rejection of common mode signals. The second gain stage consists of M6 in a common source configuration with M7 as a constant current source load. The compensation capacitor Cc is used to provide the necessary gain rolloff for stability and is connected across the second stage for the Miller multiplication effect. (For a discussion of the basic blocks which make up the amplifier see [1]).

2.2 Performance parameters

The op amp is designed to meet a number of performance specifications. The following section defines these parameters, describes their significance and gives their design equations corresponding to the two stage architecture.

2.2.1 Gain

As mentioned in chapter 1 the op amp connected in a negative feedback configuration offers many advantageous characteristics. It is important that the gain of the op amp is high as these characteristics

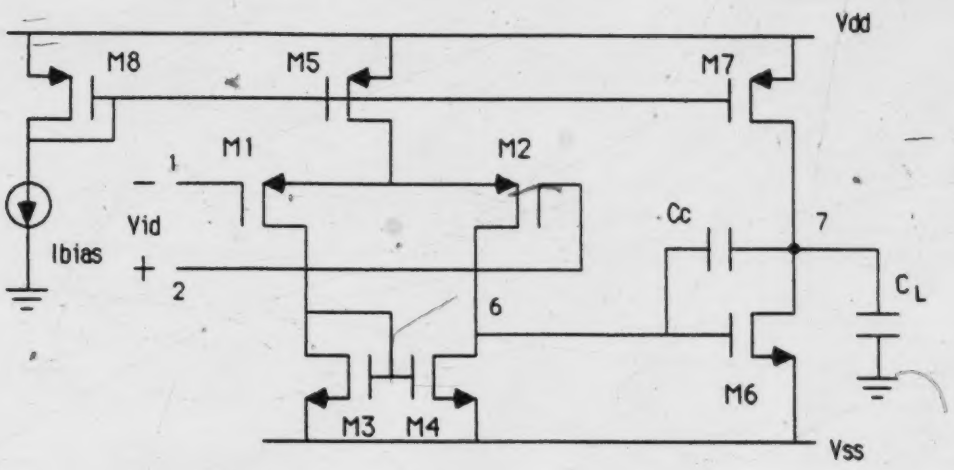


Figure 2.1 Two stage architecture

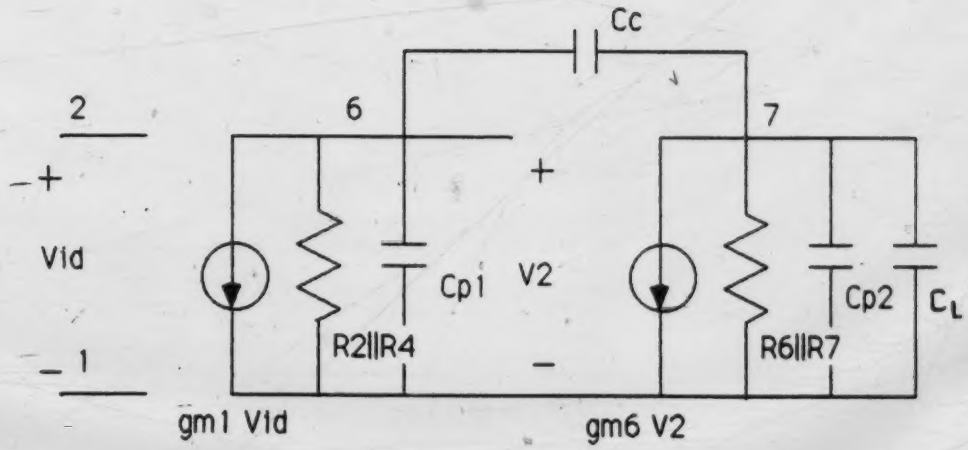


Figure 2.2 Small signal model of two stage OA

will more closely approach the ideal as the gain increases. The small signal model of figure 2.2 can be used for calculating the DC gain to be [1, p. 742]:

$$Av(0) = (g_{m1} R_{24}) (g_{m6} R_{67}) \tag{2.1}$$

where the subscripts refer to the transistor designations of figure 2.1 and $R_{24} = R_2||R_4$, $R_{67} = R_6||R_7$. The output impedance of each transistor is dependent on bias current I and device length [1] i.e.

$$R = \frac{1}{I\lambda} \quad \text{where } \lambda = \frac{1}{L_{eff}} \frac{dX_d}{dV_{DS}} \tag{2.2}$$

and $\frac{dX_d}{dV_{DS}}$ is a factor dependent on V_{DS}. (λ is typically 0.01 V^{-1} for for NMOS and 0.03 V^{-1} for PMOS).

2.2.2 Gain-Bandwidth product (GBW)

Figure 2.3 shows the op amp's frequency response characteristic based on the small signal model of figure 2.2. This characteristic is close to the usually required fully compensated OA characteristic. The dominant pole p_1 can be shown [1, p. 549] to be set by the compensation capacitor as follows:

$$p_1 \simeq -\frac{1}{(g_{m6} R_{67}) Cc R_{24}} \tag{2.3}$$

(2.3) shows that the compensation capacitor, multiplied by the gain of the second stage, is seen in parallel with the first stage output impedance. The gain thus rolls off by 3dB at p_1 and continues to roll off at a -20dB/decade rate for higher frequencies. It can be shown [12] that the gain-bandwidth product for a noninverting feedback configuration is equal to the GBW of the op amp itself. Hence this

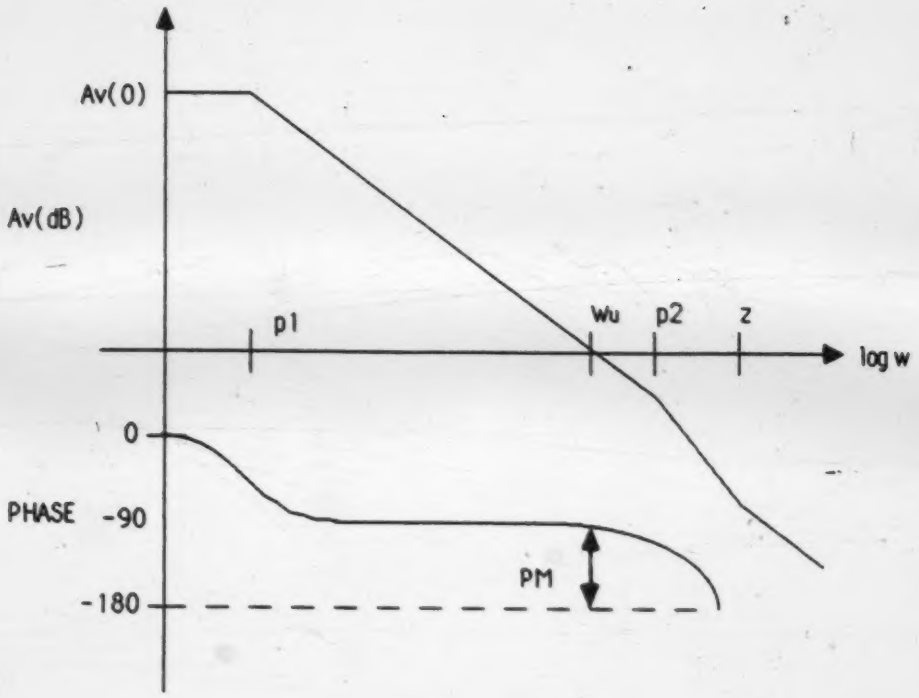


Figure 2.3 Frequency Response

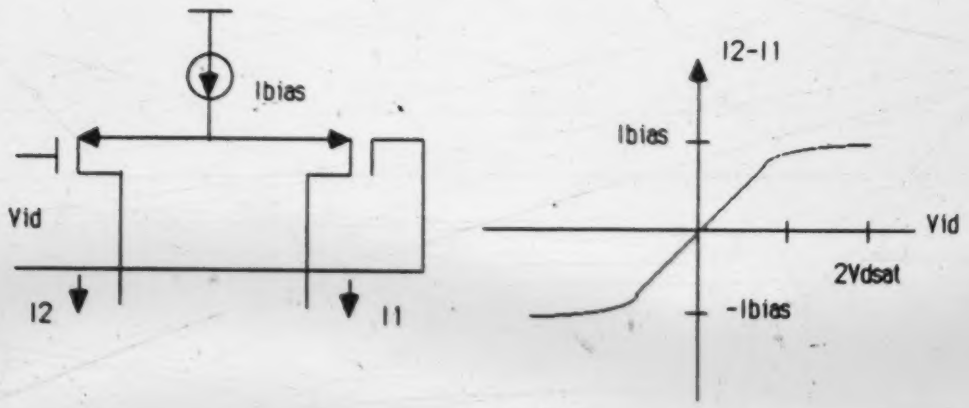


Figure 2.4 Differential pair transfer function

figure of merit is useful for calculating the bandwidth of the feedback circuit depending on the overall gain. From (2.2) and (2.3) the GBW of the two stage op amp is seen to be:

$$GBW = Av(0)p_1 = \frac{g_{m1}}{Cc} \tag{2.4}$$

It should also be noted that in the interval where the op amp gain rolls off at 20dB/decade its gain-frequency product is constant. Hence the unity gain-frequency w_u is equal to the GBW.

2.2.3 Phase margin (PM)

For stable operation in a feedback configuration the phase shift of the op amp must be sufficiently less than 180^o at the unity gain frequency. This phase margin is indicated on figure 2.3 and is usually required to be at least 45^o (preferably 60^o) to avoid excessive ringing and provide acceptable settling times. The phase margin is degraded by the nondominant pole p_2 and the right hand plane zero z. From the small signal model of figure 2.2 p_2 and z are derived as [1, p. 549]:

$$p_2 = -\frac{g_{m6}}{C_L} \tag{2.5}$$

$$z = \frac{g_{m6}}{Cc} \tag{2.6}$$

(under the assumptions $Cc, C_L \gg Cp_1$).

From (2.6) and (2.4), the location of the zero relative to w_u is given by

$$\frac{z}{w_u} = \frac{g_{m6}}{g_{m1}} \tag{2.7}$$

Thus the phase margin degradation due to the RHP zero is dependent on this transconductance ratio. Taking this into account, for a 60° phase margin the required location of p_2 relative to w_u can be approximated by:

$$\frac{|p_2|}{w_u} = \frac{1}{\tan[30 - \tan^{-1}\left(\frac{g_{m1}}{g_{m6}}\right)]} \tag{2.8}$$

This is plotted in figure 2.5. From the figure, one sees that with

$$\frac{|p_2|}{w_u} \simeq 3 \tag{2.9}$$

a 60° phase margin should be guaranteed for values of $\frac{g_{m6}}{g_{m1}} \geq 6$. However, this required value of $|p_2|/w_u$ may have to be increased in order to account for additional phase shift introduced by parasitics in the first stage which have not been considered in the approximate analysis.

2.2.4 Slew Rate (SR)

The slew rate limit of the op amp is the maximum rate of change of its output voltage. For large input signals the input differential stage leaves its linear operating region and appears as a constant current source of value Ibias (see figure 2.4). As shown in figure 2.6, the second stage with compensation capacitor will integrate this current and result in a varying output voltage of slope

$$\frac{dVo}{dt} = \frac{Ibias}{Cc} = SR \tag{2.10}$$

The slew rate must be high enough to ensure a fast settling response to large input steps when the op amp is used in pulse mode. Also, the slew rate will limit the maximum output amplitude of a sine wave for a given frequency [21].

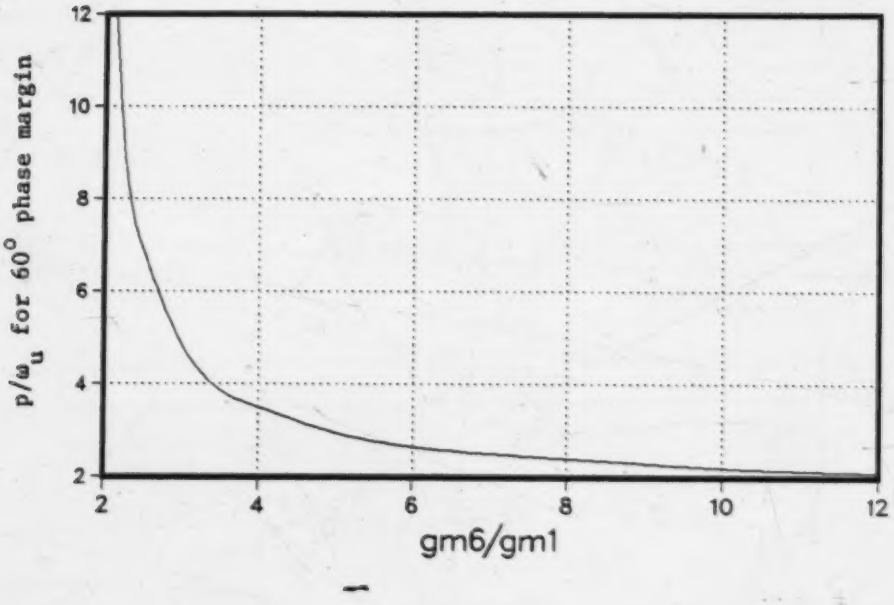


Figure 2.5 Effect of transconductance ratio on required nondominant pole location

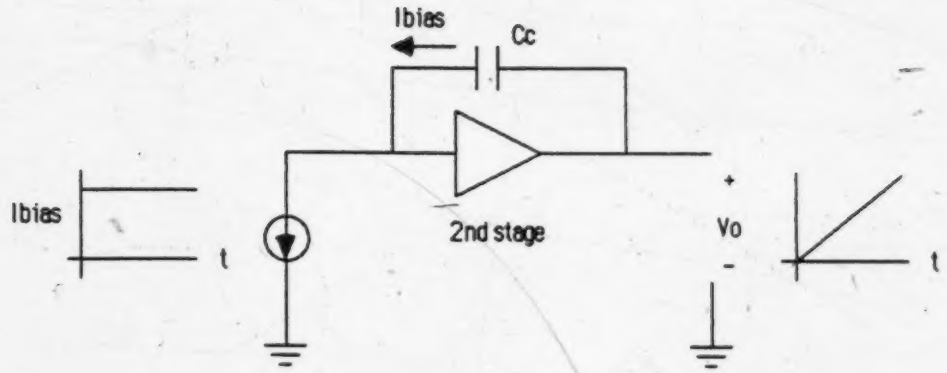


Figure 2.6 Model for calculating SR

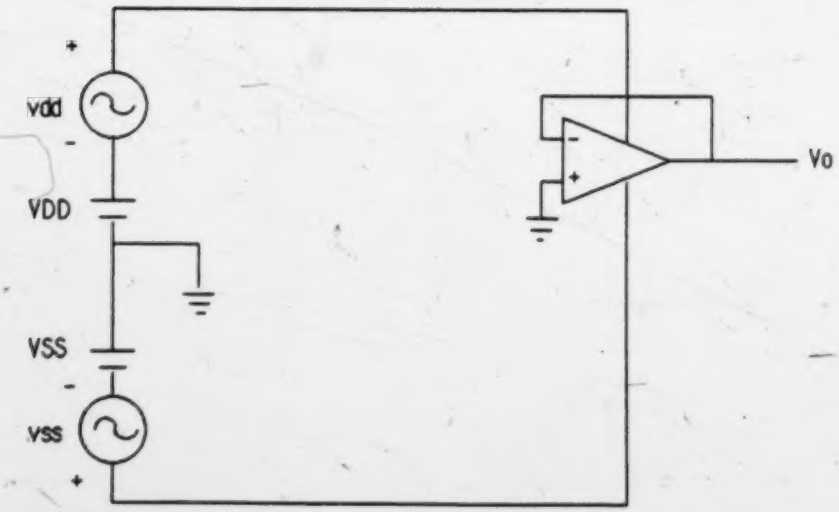


Figure 2.7 Circuit configuration for testing PSSR

2.2.5 Settling time (t_S)

The settling time refers to the time required for the op amp in a feedback configuration to settle to within a certain error band of its final output level in response to a step input. Settling times referred to in this thesis will be for a unity gain noninverting feedback configuration and an error band of 0.1%. This is the level of accuracy deemed suitable for switched capacitor signal processing applications [2]. Fast settling is very important for this application as it will set the limit on the upper frequency range of the signals to be processed.

The step response for a feedback configuration will start with a slewing period and end with the op amp in linear operation. Hence both the GBW and SR will have an effect on the settling time. Under the assumption of an OA with an integrator frequency response, the period of linear operation gives exponential settling. Under these conditions, an estimate of the GBW and SR requirements for a given t_S and voltage step can be derived (see appendix 1).

The results for a one volt step are summarized on the graphs of figure 2.8. The different curves correspond with different values of V_{DSAT} for the input transistor pair (note that V_{DSAT} must be kept low for low offset - see section 2.2.9). For a 1 V step, the exponential settling model shows the optimum value of V_{DSAT1} to be about 162 mV.

The actual settling time will be longer than predicted by the model due to the ringing caused by the nondominant pole and zero. For an OA with 60° phase margin the settling time for a 1 V step has been seen to be typically 20% longer than predicted (see table 3.1).

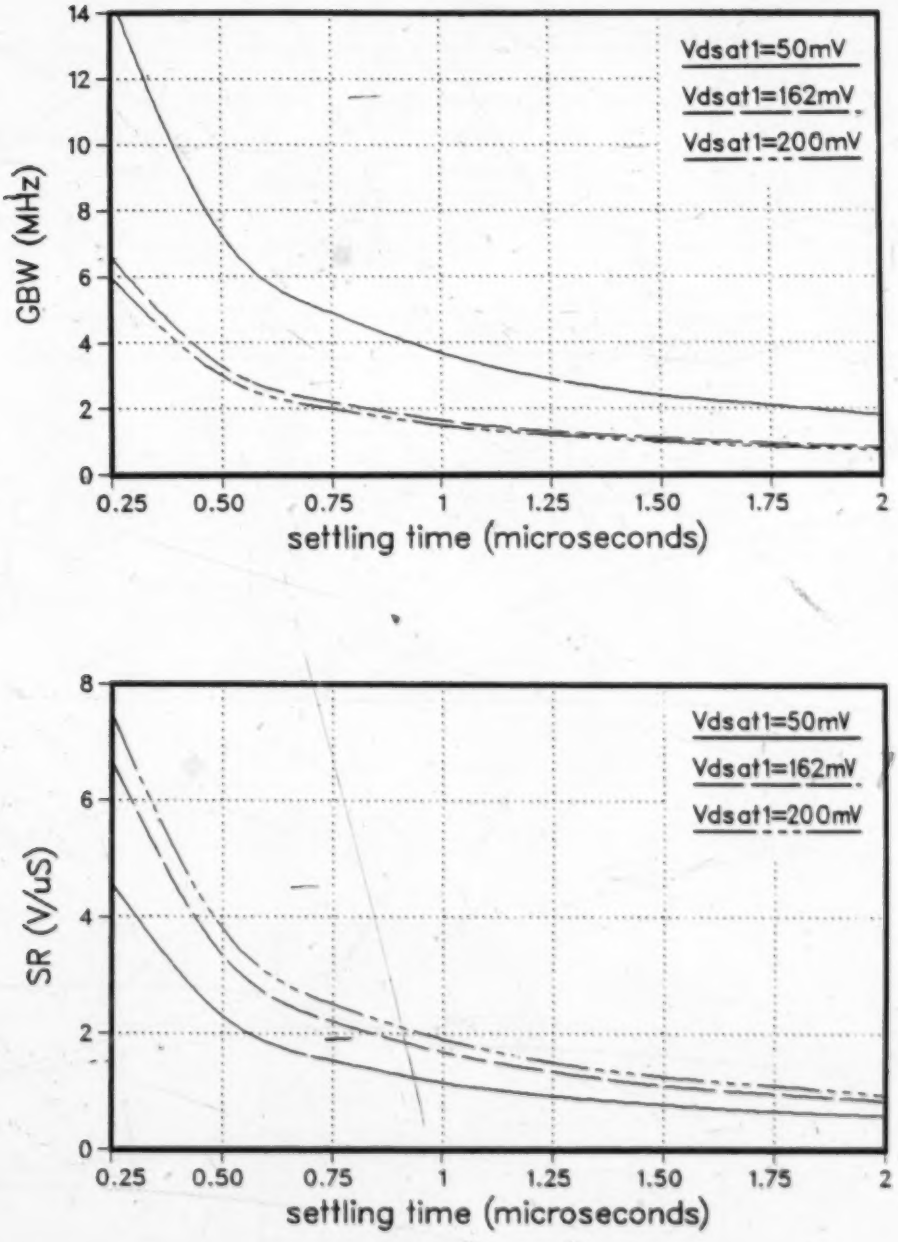


Figure 2.8 Required GBW and SR for a given settling time ts.

2.2.6 Input common mode range (ICMR) and output swing (OS)

Both these specifications define the operating range of the op amp, outside of which its characteristics become degraded. As a common mode input signal approaches V_{SS}, M1 and M2 will eventually leave pinchoff causing the gain to drop. Similarly, as the output voltage approaches V_{SS}, M6 will eventually leave pinchoff with the same result. It can be shown (appendix 2) that the -ICMR and -OS specs set upper limits on V_{DSAT3} as follows:

$$(\text{-ICMR}): \quad V_{DSAT3} \leq (Vi_{min} - V_{SS}) - |V_{t3}| + |V_{t1}| \tag{2.11}$$

$$(\text{-OS}): \quad V_{DSAT3} \leq (Vo_{min} - V_{SS}) \tag{2.12}$$

The output swing requirement will normally take precedent as body effect causes $|V_{t1}| > |V_{t3}|$ by 1 V typically. (2.11) can thus easily be met with $Vi_{min} = V_{SS}$ i.e. -ICMR extends to V_{SS}. The aspect ratio of M3 and M4 is then:

$$(W/L)_3 \geq \frac{I_5}{K_n' (V_{DSAT3max})^2} \tag{2.13}$$

A positive going common mode input eventually causes M5 to leave pinchoff causing first stage bias current to roll off and the SR to be degraded. A positive going output signal eventually causes M7 to leave pinchoff. Now +ICMR and +OS set limits on V_{DSAT5} as follows (appendix 2):

$$(\text{+ICMR}): \quad V_{DSAT5} \leq (V_{DD} - Vi_{max}) - |V_{GS1}| \tag{2.14}$$

$$\leq (V_{DD} - Vi_{max}) - \left[\sqrt{\frac{I_5}{Kp'(W/L)_1}} + |V_{t1}|\right]$$

$$(\text{+OS}): \quad V_{DSAT5} \leq (V_{DD} - Vo_{max}) \tag{2.15}$$

Once $V_{DSAT5max}$ is decided $(W/L)_5$ is found:

$$(W/L)_5 \geq \frac{2\ I_5}{K_p'(V_{DSAT5max})^2} \qquad (2.16)$$

From (2.14) above, it is seen that the +ICMR falls short of V_{DD} by at least V_{GS1}, (~ 1.2 V typically for V_t = 0.9 V). Also, to avoid an unreasonably large value of $(W/L)_5$, V_{DSAT5} cannot be chosen too small. Thus +ICMR can only be within 1.5 - 2 V of V_{DD}.

2.2.7 Power supply rejection ratio (PSRR)

The PSRR is a measure of the ability of the op amp connected in a feedback configuration to reject signals on the power supplies. This parameter is quite important for CMOS op amps since they are likely to operate in a system which combines both analog and digital circuitry on the same chip. For a configuration such as in figure 2.7 the component of Vo due to either vdd or vss (ripple on the power supply lines, say) can be shown [15] to be given by:

$$\frac{vo}{vdd} = \frac{Av_{DD}}{Av} \qquad \frac{vo}{vss} = \frac{Av_{SS}}{Av} \qquad (2.17)$$

for frequencies up to the unity gain frequency. Here Av_{DD} and Av_{SS} are the gains to the output from the power supplies. Hence the rejection ratios are defined as:

$$+PSRR(f) = \frac{Av(f)}{Av_{DD}(f)} \quad \text{and} \quad -PSRR(f) = \frac{Av(f)}{Av_{SS}(f)} \qquad (2.18)$$

For the two-stage architecture of figure 2.1 the +PSRR will typically be much higher (say 20dB) than the -PSRR. Also it remains flat out to higher frequencies before beginning to roll off. The explanation follows.

Because the diode connected transistor M3 is biased at a constant current, its drain will track V_{SS}. Since the currents in M3 and M4 are equal and their gate voltages are equal, their drain voltages must also be equal hence the first stage output will also track V_{SS}. The model of figure 2.9 can then be used to derive $Av_{SS}(w)$ shown in figure 2.10. At low frequencies, the circuit simplifies to the voltage divider R_6 and R_7. As the frequency approaches the dominant pole of the OA, the compensation capacitor acts as a short, M6 looks like a diode connected transistor and the supply signal appears almost undiminished at the output. The result is that -PSRR(w) follows Av(w) quite closely, as shown in figure 2.11.

The +PSRR can be calculated using the model of figure 2.12. The DC gain from the positive supply can be shown to be

$$Av_{DD}(0) = \frac{R_6}{R_6+R_7} - g_{m6}\,(R_6||R_7)\,T_1 \qquad (2.19)$$

where T_1 is the transfer function to the output of the first stage and can be shown to be approximately:

$$T_1 \approx \frac{1}{2\,g_{m3}\,R_5} \qquad (2.20)$$

(2.19) shows that the output of the first stage actually helps to cancel the output component due to the resistance divider R_6 and R_7. Hence the noninfinite rejection of the first stage can cause +PSRR(0) to be much higher than -PSRR(0). However (2.20) does not take into account 1st stage device mismatches and in fact T_1 can be much larger than expected. Hence the second component of (2.19) may predominate causing the +PSRR to be degraded.

$Av_{DD}(w)$ as shown in figure 2.13 can be derived from the model of

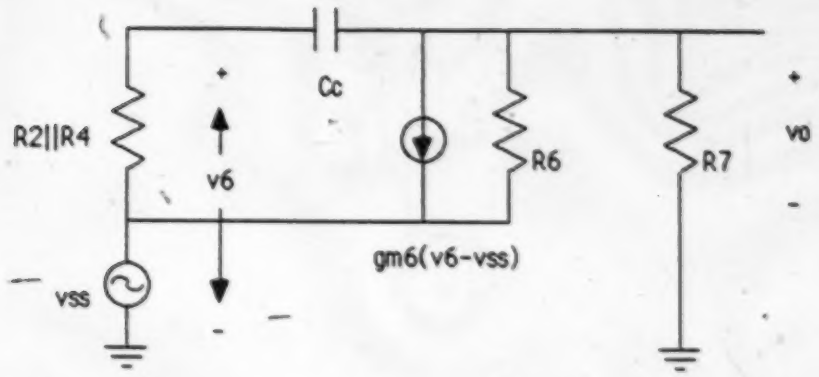


Figure 2.9 Model for -PSSR calculations

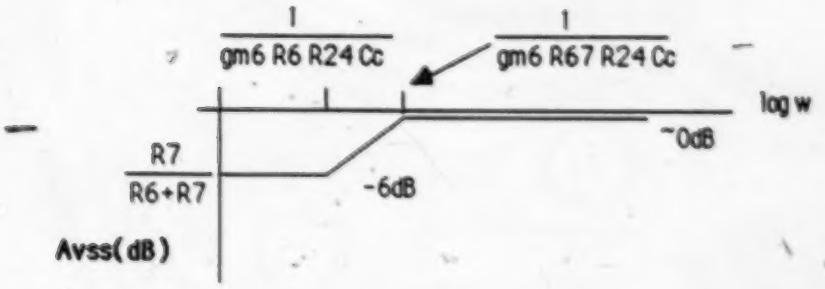


Figure 2.10 Frequency response from negative supply

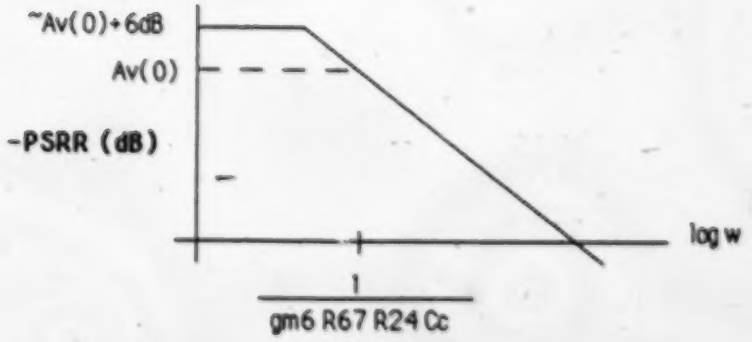


Figure 2.11 Negative PSRR

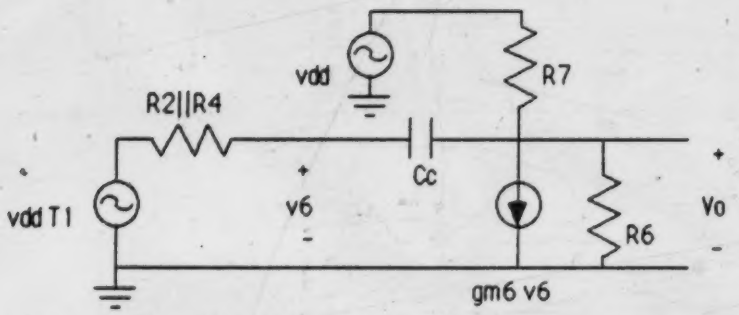


Figure 2.12 Model for +PSSR calculations

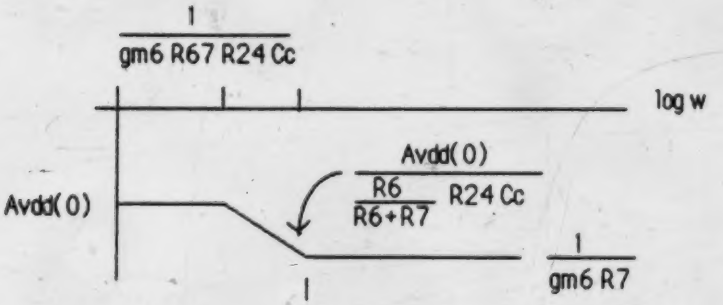


Figure 2.13 Gain from positive supply

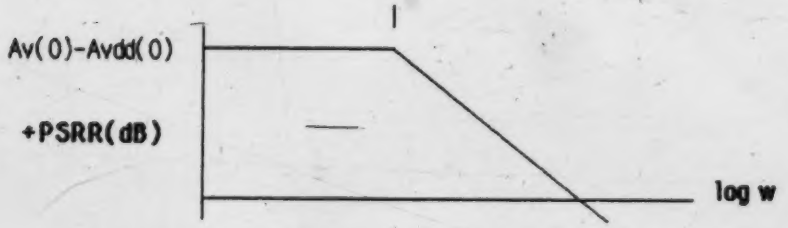


Figure 2.14 +PSRR(w)

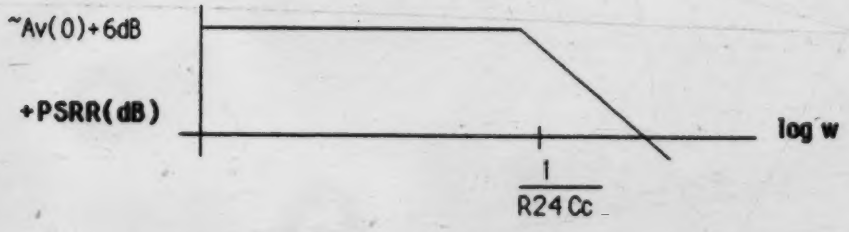


Figure 2.15 +PSRR(w) assuming infinite first stage rejection.

figure 2.12. At high frequencies Cc appears as a short causing the dominant output component to be due to the resistance divider consisting of the diode connected transistor ($1/g_{m6}$) and R_7. The frequency of which this occurs is seen to be greater than the dominant pole of the op amp. +PSRR(w) is then as shown in figure 2.14. From (2.19) it is seen that if the first stage had infinite rejection +PSRR would be approximately equal to -PSRR at low frequencies. However it would remain flat to much higher frequencies as shown in figure 2.15.

In summary then, the +PSRR is superior to the -PSRR mainly because as the frequency increases and Cc makes M6 appear as a diode connected transistor, the gain from the positive supply will roll off while the gain from the negative supply increases. If the complementary architecture with NMOS inputs were used the -PSRR would be superior as the diode connected transistor would then be the one connected to the positive supply.

2.2.8 Common mode rejection ratio (CMRR)

The CMRR is defined as:

$$CMRR = \frac{Av}{Acm} \tag{2.21}$$

where Acm is the gain for a common mode signal at the op amp inputs. This parameter is especially relevant to applications involving a noninverting feedback configuration. A unity gain buffer, for example, with input v_{cm} has an output error:

$$\frac{v_o - v_{cm}}{v_{cm}} \simeq \frac{1}{CMRR} - \frac{1}{Av} \tag{2.22}$$

hence the importance of the high CMRR.

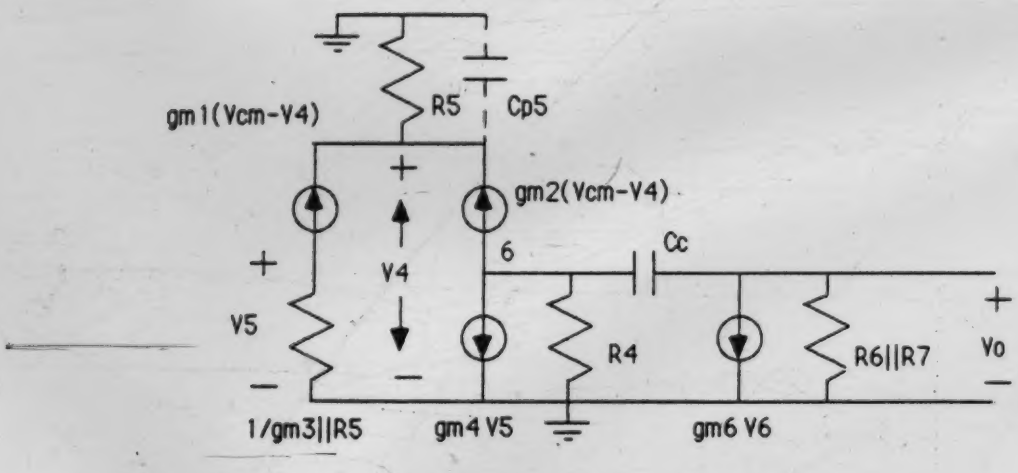


Figure 2.16 Model for CMRR calculation

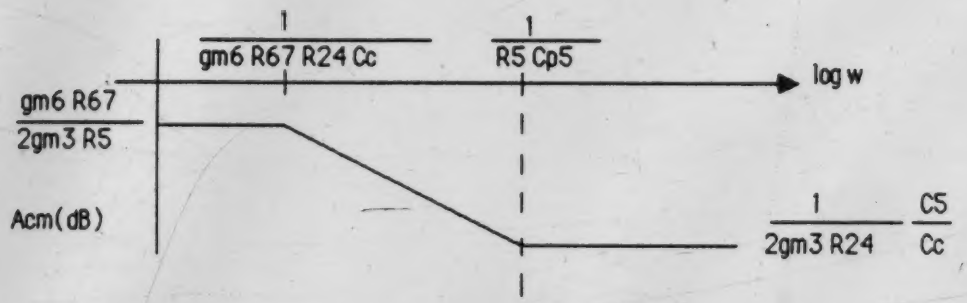


Figure 2.17 Common mode gain frequency response

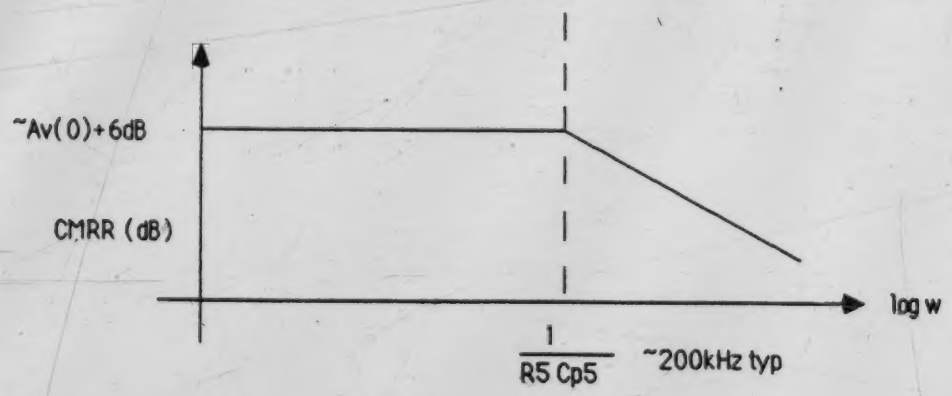


Figure 2.18 CMRR frequency response

The model of figure 2.16 can be used to calculate the CMRR of the 2 stage architecture. The DC transfer functions to the first stage output can be shown to be:

$$\frac{v_6}{v_{cm}} \simeq -\frac{1}{2g_{m3}R_5} \tag{2.23}$$

and the overall common mode gain at DC:

$$Acm(0) = \frac{v_7}{v_{cm}} \simeq \frac{g_{m6}R_{67}}{2g_{m3}R_5} \tag{2.24}$$

which can be typically -6dB.

The overall rejection can be improved by increasing the transconductance of the current mirror load and by increasing the length of M5.

The frequency response of Acm is set by Cc which introduces a low frequency pole and the parasitic Cp_5 associated with source-substrate capacitance which by shunting M5 introduces a high frequency zero. The result is as shown in figure 2.17. Because Acm rolls off at the dominant pole frequency of the op amp, the CMRR will stay flat out to quite high frequency (see figure 2.18).

2.2.9 Voltage offset and noise

With no input signal, a voltage offset and noise appear at the op amp output. The voltage offset can be considered a type of low frequency noise as it drifts with time (aging), temperature or supply voltage. The effect of these additive error sources on an operational circuit can be modelled by using equivalent input sources in series with the terminals of a noiseless and offset-free op amp as shown in figure 2.19.

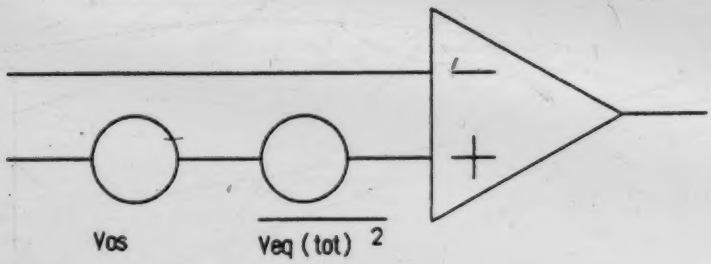


Figure 2.19 Representaion of offset voltage and noise

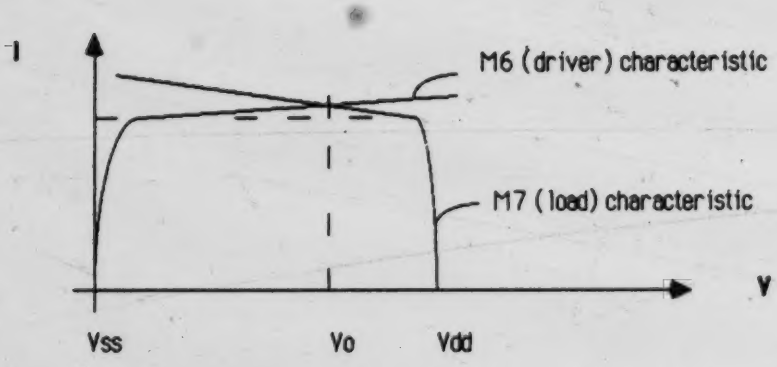


Figure 2.20 Second stage operating point

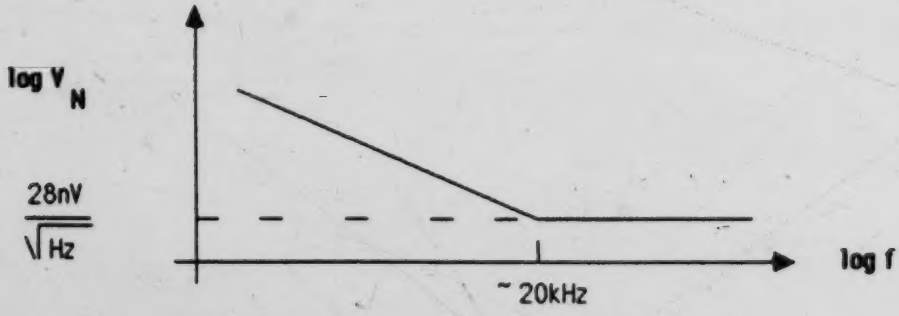


Figure 2.21 Spectral noise density example

Vos is defined as the differential input voltage (with zero common mode voltage) required to force the output voltage to be zero. For the two stage architecture, the offset can be divided into systematic and random contributions. The systematic contribution results from an imbalance in the bias currents of M6 and M7. Roughly speaking the gate voltage of M6 must be set such that the current of M6 takes up all the current of M7. This sets the following requirement on the W/L ratios:

$$\frac{(W/L)_6}{(W/L)_3} = 2\,\frac{(W/L)_7}{(W/L)_5} \tag{2.25}$$

In actual fact this will still result in some imbalance due to the different output impedances of PMOS (M7) and NMOS (M6) devices. Figure 2.20 shows the output voltage as the intersection of the characteristic curves of the output devices. It can be seen from the figure that because the PMOS device has typically 1/3 the output impedance of the NMOS device either the M6 characteristic must be raised or the M7 characteristic lowered to bring Vo midway between V_{DD} and V_{SS}. This corresponds to slightly increasing $(W/L)_6$ relative to $(W/L)_3$ or decreasing $(W/L)_7$ relative to $(W/L)_5$. These adjustments can be made during computer simulation. In practical terms the adjustment is usually not required as the resulting input offset is typically less than 1 mV.

The random offset component is due to threshold mismatches or W/L mismatches and is usually on the order of several mV. It can be shown [1, p. 745] to be given by:

$$Vos = \Delta V_{t(1-2)} + \Delta V_{t(3-4)}\,\frac{g_{m3}}{g_{m1}} + \left(\frac{I}{g_M}\right)_{(1-2)}\left[\left(-\frac{\Delta W/L}{W/L}\right)_{(1-2)} - \left(\frac{\Delta W/L}{W/L}\right)_{(3-4)}\right] \tag{2.26}$$

The contribution due to the threshold mismatch of the current mirror load is minimized by having a small g_{m3}/g_{m1}. The W/L mismatch contribution is reduced by having a small I/g_M ratio. This is ensured by operating the input transistors with $(V_{GS}-V_t) \simeq 50\text{-}200$ mV.

The equivalent input noise voltage Vn can also be shown [1, p. 750] to be predominantly due to the inherent noise of the input pair if g_{m1} is made 2 or more times greater than g_{m3} and L_3 is made 2 or more times greater than L_1. The input noise spectral density will then be:

$$\frac{\overline{v_N^2}}{\Delta f} = \frac{2KF_p}{fW_1L_1Cox} + 4kT\left(\frac{4}{3g_{m1}}\right) \qquad (2.27)$$

The first component is the 1/f or flicker noise and can be minimized by increasing the device area. The noise coefficient KF is strongly process dependent and is typically 2 or 3 times smaller for the PMOS as opposed to the NMOS device. The second component is due to thermal noise and can be reduced by increasing g_{m1}.

A typical value for KF_p might be 3×10^{-12} V^2pF [1]. Figure 2.21 then shows the spectral noise density for an 80 x 10 micron device (see design example) assuming $KF_p \simeq 3\times10^{-12}$ V^2pF, $Cox \simeq .4$ $fF/\mu m^2$, $I \simeq 5$ μA, and $K_p' = 10$ $\mu A/V^2$. Note that the flicker noise is dominant up to about 20 kHz.

To calculate the total equivalent input noise voltage for an operational circuit requires integration of the spectral density function (2.27) over the frequency range. For the above example, if the op amp is connected as a unity gain buffer and $f_u \simeq 1$ MHz the total noise voltage is calculated to be $Vn \simeq 40$ μV. This sets

the lower limit on the minimum signal size which can be applied to the circuit.

2.3 Typical Performance Parameters

Table 2.1 gives the expected performance specifications for a two-stage CMOS internal op amp with PMOS inputs. Achievable performance in the areas of GBW, SR, die area and P_{diss} is highly dependent on C_L. This will be further appreciated in the design example.

2.4 Design

2.4.1 Procedure

For simplicity, the op amp is designed to meet the following set of "primary" design specifications: PM, SR, GBW, ±ICMR, ±OS. The "secondary" specifications of Av(0), CMRR, PSRR, t_S and P_{diss} are then checked (usually by computer simulations) to see if they are acceptable. If they are not acceptable, it may be that the primary set of specifications is incompatible and needs to be revised. For instance, it can be shown [13, p. 225] that Av(0) and CMRR are fully determined by the GBW and SR. Similarly, t_S and P_{diss} are both determined by SR, GBW and PM.

The list of design equations corresponding to the architecture of figure 2.1 is given in table 2.2. The order of calculations is summarized in the flowchart of figure 2.22. Bold items indicate performance parameters while items in square boxes are the final circuit values.

SPEC	TYPICAL VALUES
Av(0)	$10^3 - 10^4$
GBW	1 - 10 MHz
SR	2 - 20 V/μs
PM	60^o
t_S	$\leq$ 1 μs (0.1%, 1 V step, C_L=5 pF)
+ICMR	V_{DD} -1.5 V
-ICMR	V_{SS}
+OS	V_{DD} -0.5 V
-OS	V_{SS} +0.5 V
+PSRR (DC)	100 dB
-PSRR (DC)	80 dB
CMRR (DC)	80 dB
OFFSET	$\leq$ 10 mV
NOISE	$\leq \frac{100\ nV}{\sqrt{Hz}}$ @ 1 kHz
P_{diss}	0.5 - 10 mW
DIE AREA	$\leq$ 100,000 micron^2
LOAD	1 - 100 pF

Table 2.1 Typical performance specifications for a 2-stage CMOS op amp (PMOS input configuration)

Performance parameter	Design equations
PM $\geq 60^{o}$	$\frac{g_{m6}}{C_L} \geq 3\, w_u^{*}$
SR	$I_5 = SR\, C_L$
GBW	$g_{m1} = GBW\, C_L$
-ICMR	$V_{DSAT3} \leq (Vi_{min} - V_{SS}) - \lvert V_{t3}\rvert + \lvert V_{t1}\rvert$
-OS	$V_{DSAT3} \leq Vo_{min} - V_{SS}$
+ICMR	$V_{DSAT5} \leq (V_{DD} - Vi_{max}) - \left(\sqrt{\frac{I_5}{Kp'(W/L)_1}} + \lvert V_{t1}\rvert\right)$
+OS	$V_{DSAT5} \leq V_{DD} - Vo_{max}$
Noise and Offset	$g_{m3} \leq 1/2\, g_{m1}$
	$L_3 \geq 2\, L_1$

Table 2.2 Design Equations

* see notes of section 2.4.1

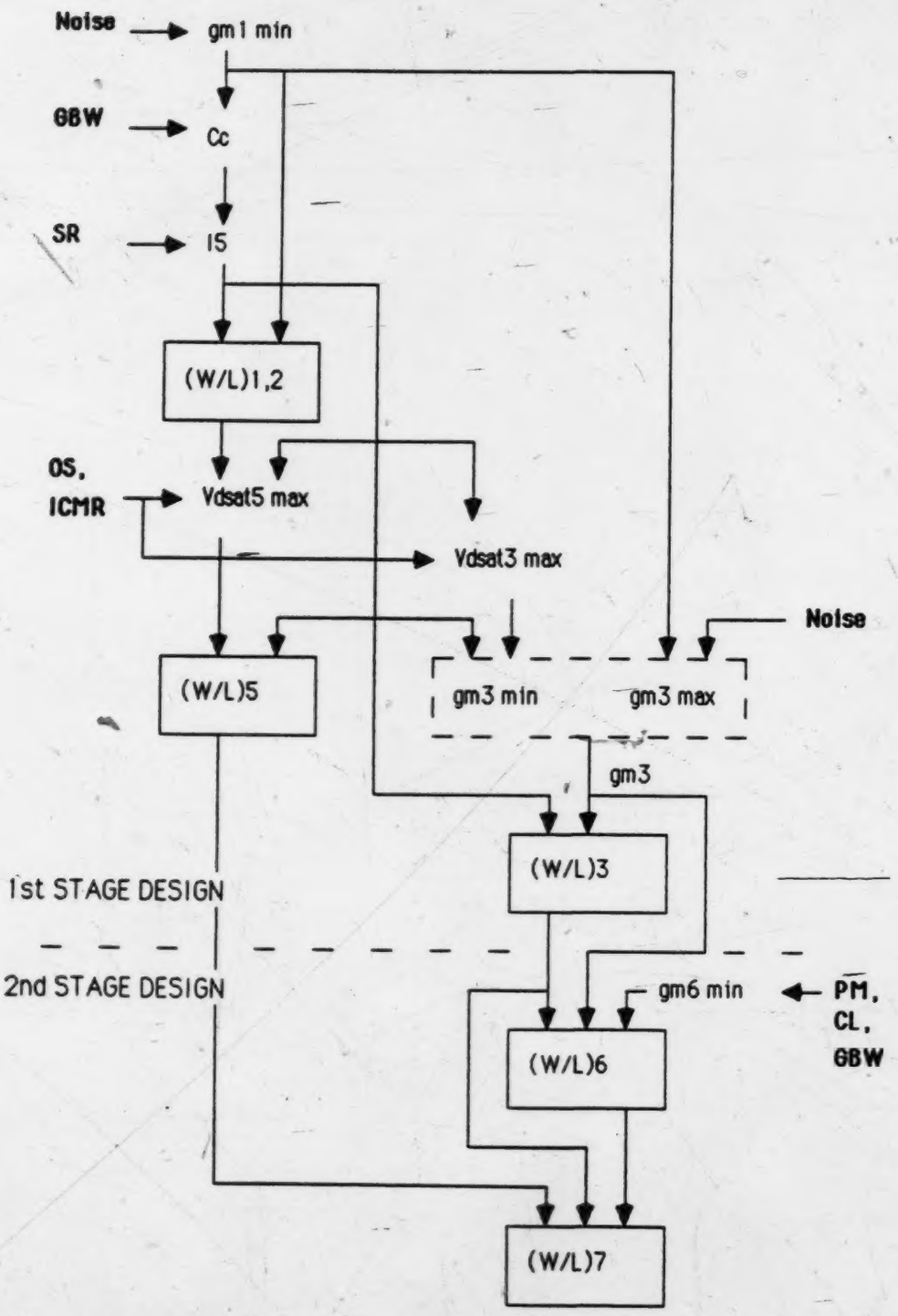


Figure 2.22 Design flowchart

Note the following:

1. It is advantageous to choose g_{m1} at the lowest limit set by thermal noise (see equation (2.27)). From (2.4) it is seen that for a given GBW, this results in the smallest value for Cc and hence reduced area requirements. Also, it means reduced P_{diss} and higher gain since a smaller first stage current is required for a given SR.

   The smaller value of g_{m1} also results in a higher frequency RHP zero. Since g_{m6} is fixed by the PM requirement (see (2.5)), a smaller g_{m1} means a larger transconductance ratio. From (2.7) then, it is seen that the RHP zero moves further from w_u resulting in an improved phase margin.

2. If a large g_{m1} is required giving $g_{m6}/g_{m1} < 6$, $p/w_u = 3$ will be insufficient for a 60^o phase margin (see figure 2.4). A compensation technique from the next chapter should be used since otherwise a large p/w_u ratio may be required resulting in much larger second stage current (see next point). An indication that $g_{m6}/g_{m1} < 6$ is given by $Cc > C_L/2$ since from (2.5) and (2.4) it can be written

$$\frac{g_{m6}}{g_{m1}} = 3\,\frac{C_L}{Cc} \tag{2.28}$$

3. For minimum second stage current the ratio g_{m3}/g_{m1} should be as large as possible. Because M3, M4 and M6 have a common gate voltage we can write:

$$I_6 = \frac{g_{m6}}{g_{m3}}\frac{I_5}{2} = \frac{g_{m6}}{g_{m3}}\frac{SR\ C}{2} = \frac{g_{m6}}{g_{m3}}\frac{SR}{2}\frac{g_{m1}}{w_u}$$

$$= (p/w_u)\ SR\ C_L\ \frac{g_{m1}}{2g_{m3}} \tag{2.29}$$

Hence from (2.29) the larger g_{m3}/g_{m1} the smaller I_6. As indicated in the design flowchart, g_{m3} usually has an upper limit of $g_{m3} = g_{m1}/2$ to prevent excess noise and offset. However if the lower limit set by ICMR and OS exceeds this, there will necessarily be some performance tradeoff. If the noise limit for g_{m3} is used and $p/w_u=3$ (2.29) becomes

$$I_6 = 3\ SR\ C_L \qquad (2.30)$$

4. From (2.2) it is seen that transistor output resistance is directly proportional to the device length. Hence the gain requirement usually sets a lower limit on the length. $L \geq 10$ micron is suggested. The length of matched devices should be equal for best matching.

2.4.2 Example

The following design example is for a conventional two stage op amp which was submitted for fabrication using Northern Telecom's 5 micron process. Test results on this op amp are given in chapter 4. Its performance was used as a benchmark against which other designs appearing in this thesis were compared. The chosen design specifications are given in table 2.3. Note that a larger than typical load capacitance was chosen because of the requirement that the op amp would have to drive off chip loads for testing.

The calculations follow the design flow of figure 2.22. Northern Telecom's process parameters were taken from [3]. All device lengths were taken as 10 micron for adequate gain and best matching. Note that to avoid accumulation of error, whenever a transistor dimension is

GBW	1 MHz
SR	2 V/μs
PM	$\geq 60^{o}$
C_L	20 pF
+ICMR	V_{DD} - 2 V
-ICMR	V_{SS}
+OS	V_{DD} -0.5 V
-OS	V_{SS} +0.5 V
Av(0)	$\geq$ 5000

Table 2.3 Specifications for the design example

rounded off to the nearest micron, the aspect ratio is recalculated for use in later calculations.

1. Phase margin requirement:

$$g_{m6(min)} \simeq 3C_L w_u \qquad (2.31)$$

$$= 3\ (20\ pF)\ (2\ \ 1\ MHz) = 377\ \mu A/V$$

g_{m6} = 355 μA/V was used in the implemented design and so is chosen here.

2. Noise requirement:

A transconductance ratio of about 10 was deemed as resulting in a satisfactory noise level. Hence g_{m1} = 27.6 μA/V corresponding with g_{m6}/g_{m1}=12.86 was chosen.

3. Gain-Bandwidth requirement:

$$Cc = \frac{g_{m1}}{GBW} = \frac{27.6\ \mu A/V}{2\pi\ (1\ MHz)} = 4.4\ pF \qquad (2.32)$$

4. Slew rate requirement:

$$I_5 = Cc\ SR = 4.4\ pF\ (2\ V/\mu s) = 8.8\ \mu A \qquad (2.33)$$

$$(W/L)_1 = \frac{g_{m1}^2}{I_5 K_p'} = \frac{(27.6)^2}{8.8\ (9.75)} = 8.88 \qquad (2.34)$$

L_1 (DRAWN) = 10 μm

L_1 (ACTUAL) = (10 - 1.2) μm = 8.8 μm

W_1 (DRAWN) = 8.88 (8.8 μm) = 78.14 $\simeq$ 78 μm

So final values are

$$(W/L)_1 = \frac{78}{8.8} = 8.86 \qquad (2.35)$$

and $g_{m1} = \sqrt{2IK_p'(W/L)_1} = \sqrt{8.8\ (9.75)\ \frac{78}{8.8}} = 27.6\ \mu A/V$

Note that to have an acceptable level of 1/f noise, W_1 and L_1 may have to be scaled up to get a larger transistor area (see section 2.2.9).

5. Negative going ICMR and OS requirement:

(-ICMR):

$$V_{DSAT3} \leq (Vin_{(min)} - V_{SS}) - V_{t3} + |V_{t1}|_{max} \tag{2.36}$$

where $V_{t1(max)} = V_{t0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$ (2.37)

$$= 0.9 + 0.634\ (\sqrt{.612 + 9} - \sqrt{.612}) = 2.4\ V$$

(here V_{SB} is estimated)

so $V_{DSAT3} \leq 0 - 0.9 + 2.4 = 1.5\ V$

(-OS):

$$V_{DSAT3} \leq Vo^-_{(max)} - V_{SS} = 0.5\ V \tag{2.38}$$

Hence the output swing requirement on V_{DSAT3} overrides and

$$(W/L)_3 \geq \frac{I_5}{K_n'(V_{DSAT3})^2} = \frac{8.8}{30\ (0.5)^2} = 1.17 \tag{2.39}$$

choose L_3 (DRAWN) = 10 μm

so L_3 (ACTUAL) = 10 - 1.4 = 8.6 μm

and W_3 (DRAWN) = 1.17 (8.6) = 10.06 μm, say 10 μm

this gives $g_{m3} = \sqrt{2I_3 K_n' (W/L)_3}$ (2.40)

$$= \sqrt{2\ (4.4)\ 30\ (1.163)} = 17.5\ \mu A/V$$

and $\frac{g_{m3}}{g_{m1}} = \frac{17.5}{27.6} = 0.63$

For noise and offset considerations this ratio should not be increased (see (2.26)) so $(W/L)_3$ cannot be increased further. (Also, in retrospect, L_3 should have been chosen $L_3 \geq 2L_1$ for reduced 1/f noise contribution from M3 and M4 [1, p. 750]. This is overlooked here in order to be in agreement with the dimensions of the circuit submitted for fabrication.

6. Knowing g_{m6}, g_{m3} and $(W/L)_3$, $(W/L)_6$ can be derived from the fact that M3 and M6 have a common gate voltage. Hence

$$\frac{g_{m6}}{g_{m3}} = \frac{\beta_6 V_{DSAT}}{\beta_3 V_{DSAT}} = \frac{W_6}{W_3} \tag{2.41}$$

if $L_6 = L_3 = 10\ \mu m$

therefore $W_6 = 10\ \frac{355}{17.5} \simeq 203\ \mu m$

7. Positive going ICMR and OS:
(+ICMR):

$$V_{DSAT5} \leq (V_{DD} - Vi_{(max)}) - \left(\sqrt{\frac{I_5}{Kp'(W/L)_1}} + V_{t1(min)}\right) \tag{2.42}$$

where $V_{t1(min)} = V_{t1(0)} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$ (2.43)

$$\simeq 0.9 + 0.634(\sqrt{.612 + .5} - \sqrt{.612})$$

$$= 1.07$$

(note: here V_{SB} is estimated)

hence

$$V_{DSAT5} \leq 2 - \left(\sqrt{\frac{8.8}{9.75(8.86)}} + 1.07\right)$$

$$\leq 2 - 1.39$$

$$\leq 0.6$$

(+OS):

$$V_{DSAT5} \leq V_{DD} - Vo^{+}_{(max)} - 0.5\ V \tag{2.44}$$

Hence the output swing requirement on V_{DSAT5} overrides.

So

$$(W/L)_5 \geq \frac{2\ I_5}{Kp'(V_{DSAT5})^2} = \frac{2(8.8)}{9.75(0.5)^2} = 7.22 \tag{2.45}$$

Choose

L_5 (DRAWN) = 10 μm

then L_5 (ACTUAL) = 10 - 1.2 = 8.8 μm

and W_5 (DRAWN) = 7.22 (8.8 μm) = 63.54 $\simeq$ 64 μm

So the final ratio is $(W/L)_5 = 64/8.8 = 7.273$

8. Systematic offset requirement:

Choose $L_7 = L_5 = 10\ \mu m$. Then because $L_6 = L_3$, (2.25) can be written

$$W_7 = W_5 \cdot \frac{1}{2} \cdot \frac{W_6}{W_3} \qquad (2.46)$$

In order to get a round number, W_6 is altered to 205 microns, then:

$$W_7 = \frac{64}{2} \frac{205}{10} = 656\ \mu m$$

9. Power dissipation request:

From (2.30) and (2.10) the total bias current can be estimated as

$$Ibias \simeq SR\ C + 3\ SR\ C_L \qquad (2.47)$$

From (2.28) this can be rewritten:

$$Ibias \simeq 3\ SR\ C_L\ (g_{m1}/g_{m6} + 1) \qquad (2.48)$$

For this design then, Ibias is

$$Ibias \simeq 3\ (2\ V/\mu s)(20\ pF)(1/12.9 + 1)$$

$$= 129\ \mu A$$

Hence with ± 5V supplies the expected power dissipation is 1.29 mW.

Simulations

The gain, CMRR and PSRR are difficult to predict due to the inaccuracy of estimating transistor output resistance. Hence it is best to use the more accurate SPICE [22] level 2 models in order to check that these performance areas are acceptable. Also, the simulations verify that the primary design specifications are met. Appendix 3 shows the basic SPICE file which was used. Transistor source and drain areas and peripheries were estimated from Northern Telecom's 5 micron design rules as shown in figure 2.23. As a result of the simulation process, the end values for the second stage

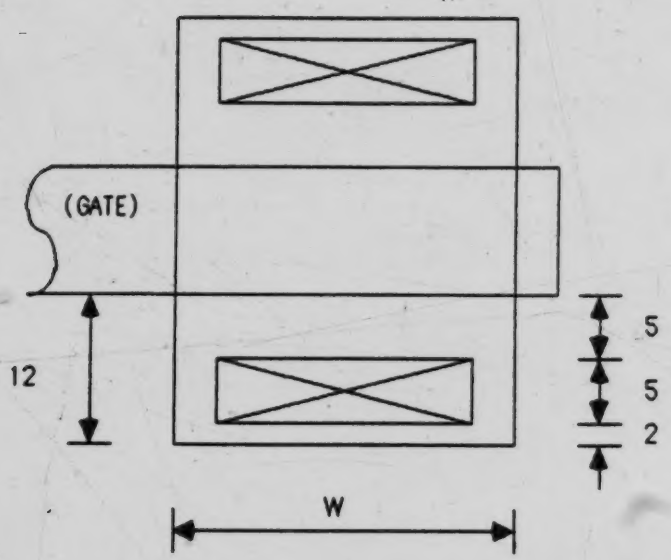


Figure 2.23 Transistor dimensions for 5 micron rules

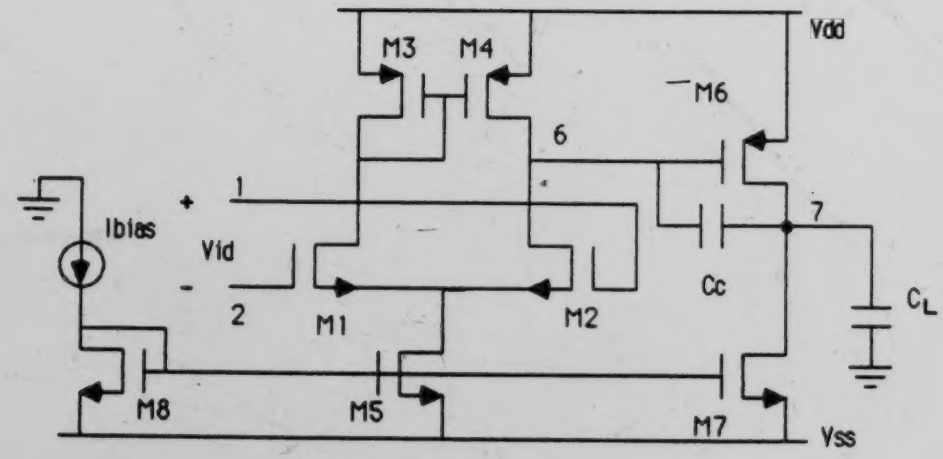


Figure 2.24 Two stage op-amp with NMOS inputs

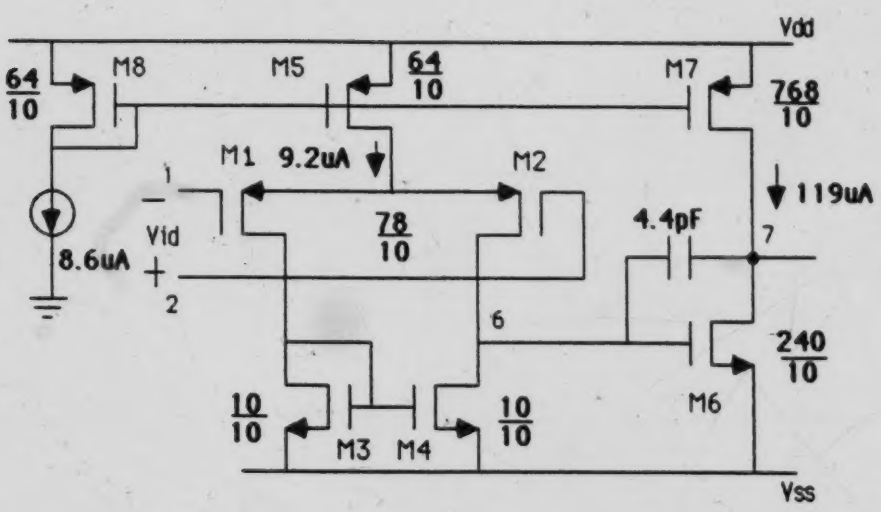


Figure 2.25 Final circuit for design example

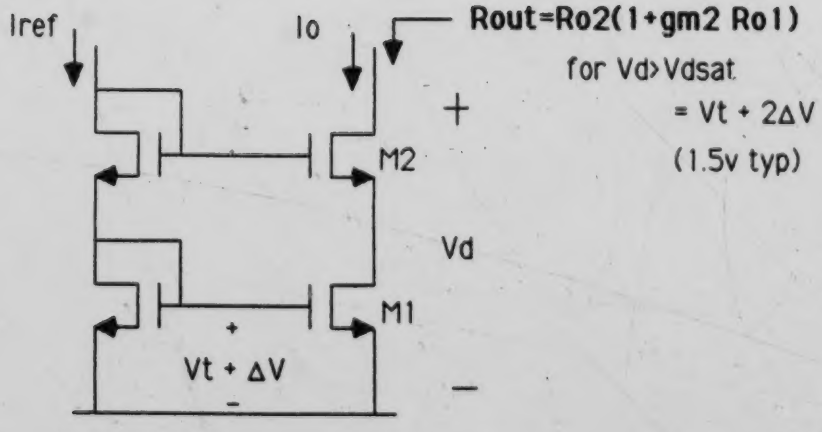


Figure 2.26 Cascoded transistor configuration

transistor sizes differs from the above design values. The final circuit is shown in figure 2.25. During the simulations, it was observed that the more accurate MOSFET model resulted in lower values of V_{DSAT} than expected. Although this meant that ICMR and OS were better than expected, it also resulted in the need to increase $(W/L)_6$ in order to obtain the desired transconductance. $(W/L)_7$ consequently also had to be increased to prevent systematic offset. A summary of all the simulation results can be found in table 3.4. Measurements of the actual circuit implementation are given in chapter 4.

2.4.3 Evaluating tradeoffs

If during the simulation phase the op amp performance is seen to be deficient in some area it will be necessary to make some circuit adjustments. To help in this process, table 2.4 shows the general relationship between the circuit parameters and the performance parameters. From the table one can see that for a given circuit change, performance in one area may improve while in another it may degrade. The designer can then choose the approach which results in the most acceptable tradeoff.

As an example of the use of the table, consider that the first stage current is increased. From the table it is seen that SR, GBW and the thermal noise level should improve. However, Av(0), ICMR, OS, PSRR, CMRR and offset will degrade. Looking across the table, though, shows that increasing the aspect ratios of M1, M2, M3, M4 and M5 will counteract these degradations while maintaining the improvements in SR, GBW and noise.

Table 2.4 Relationships between cct and performance parameters

(See notes in section 2.4.3)		1st stage current	M1 and M2		M3 and M4		M6		M7		M5		Cc	Cl
		I5	W/L	L	W/L	L	W/L	L	W/L	L	W/L	L		
Increase	Av (0)	↓	↑2	↑3	↑2*	↑3		↑3	↓2*	↑3				
Increase	GBW	↑2	↑2										↓	
Increase	P2/Wu		↓2				↑2						↑	↓
	Z/Wu		↓2				↑2							
Increase	SR	↑											↓	
Increase	-ICMR	↓2			↑2									
	- OS	↓2			↑2									
Increase	+ICMR	↓3	↑3								↑2			
	+ OS	↓2									↑2			
Increase	PSRR	↓	↑2	↑3		↑3		↑3		↑3				
Increase	CMRR	↓	↑2	↑3	↑2	↑3						↑		
Decrease	Offset	↓3	↑3	↑3	↓3	↑3								
Decrease	$\frac{1}{f}$ noise		↑3	↑3	↓3	↑3								
Decrease	thermal noise	↑3	↑3		↓3									
Decrease	Area												↓3	
Decrease	Pdiss				↑+		↓*		↓*+					

Notes:

1. In changing one circuit parameter care must be taken that the other circuit parameters remain constant. For instance if we wish to increase Av(0) by increasing L_1 and L_2 then W_1 and W_2 must be proportionately increased to maintain W/L constant.
2. Note 2 indicates a square root relationship.
   i.e. $Av(0) \alpha \ 1/\sqrt{I_5}$
3. Note 3 indicates a circuit parameter which does not show a proportional relationship with the performance parameter.
4. * and + indicate circuit parameters which are coupled and can only be changed by the same factor. For example in note 3 of section 2.4.1 it is shown that I_2 can be decreased if g_{m3} is increased. Hence in the table for reducing power dissipation $(W/L)_7$ can be decreased if $(W/L)_3$ is simultaneously increased by the same factor.
5. 2nd stage current does not appear as a separate circuit parameter since it is set by the relative sizes of $(W/L)_6$ to $(W/L)_3$ and $(W/L)_7$ to $(W/L)_5$.

2.4.4 NMOS vs PMOS inputs

The two stage design can be implemented using a complementary architecture which has an NMOS instead of PMOS input pair as shown in figure 2.24. With the NMOS devices there is the choice of connecting the source and body (p-well) together or leaving them separate (p-well connected to V_{SS}). Connecting them together prevents body effect from altering v_6. However, in the case of a differential pair, body effect is actually beneficial. For one polarity of common mode input

it causes $|V_{t1}|$ to increase resulting in an extended ICMR (see (2.11)). Also, it does not degrade the differential gain of the stage, since for balanced inputs the input pair sources are at AC ground. As for the common mode gain, it can be shown to be actually reduced by a factor of $\frac{g_{m1}}{g_{m1} + g_{mb1}}$ resulting in a ~ 1dB improvement in CMRR.

However, one case in which being able to connect source and body together is beneficial is in reducing power supply coupling to the output at high frequencies due to "supply capacitance" [2]. If the body effect is present, power supply variations cause V_{GS} variations on the input pair. With the op amp connected in a feedback configuration, the resulting capacitance currents due to the gate parasitic flow in the feedback path causing an output voltage variation.

For the NMOS input configuration, the source of the second stage driver is connected to V_{DD}. Hence the +PSRR can be expected to be much worse than the -PSRR (see section 2.2.7). Also, since the first stage bias source M5 is next to V_{SS} the -ICMR can be expected to be much less than the +ICMR (see section 2.2.6). This is vice versa for the PMOS input configuration.

Finally, the equivalent input noise source for the NMOS input configuration can be expected to be higher by a factor of typically 3X [1]. This is due to the process dependence of 1/f noise.

Table 2.5 compares the typical performance of the NMOS input (with and without source-body connection) and the PMOS input configurations.

	NMOS*	NMOS+	PMOS
+ICMR	V_{DD} -0.5 V	V_{DD}	V_{DD} -1.5 V
-ICMR	V_{SS} +1.5 V	V_{SS} +1.5 V	V_{SS}
+PSRR (DC)	76 dB	76 dB	90 dB
-PSRR (DC)	90 dB	90 dB	76 dB
1/f noise			3x NMOS

* with source - body connected
\+ without source - body connected

Table 2.5 Comparison of NMOS vs PMOS input configurations

2.5 Effects of different architectures

Several modifications to the two-stage architecture and several alternate architectures have been used to improve on some aspects of performance.

2.5.1 Variations of the two-stage

For the two-stage design, improved phase margin can be achieved by using a resistor [4] or a buffer [5] in series with the compensation capacitor. (This is elaborated on in chapter 3). Also, the PSRR of the two-stage can be improved by the insertion of a cascode device in series with the compensation capacitor [2].

The gain of the two-stage OA can be improved by the use of cascoded transistors. The cascode configuration (figure 2.26) has a much higher output impedance, typically 50X greater than a normal transistor. By incorporating this configuration in the 1st or 2nd stage of the OA very high gains (> 100dB) can be achieved although the phase margin can become degraded and the compensation becomes more complicated [6]. Another problem with the cascode configuration is the increased value of V_{DSAT} (see figure 2.26) which limits the linear operating range. With a cascoded first stage the ICMR will be reduced which is not a problem for an inverting amplifier configuration but will be for a buffer. With a cascoded second stage the output swing becomes reduced. This problem can be alleviated by using special biasing techniques [1, p. 715]. Figure 2.27 shows an op amp with a cascoded 1st stage.

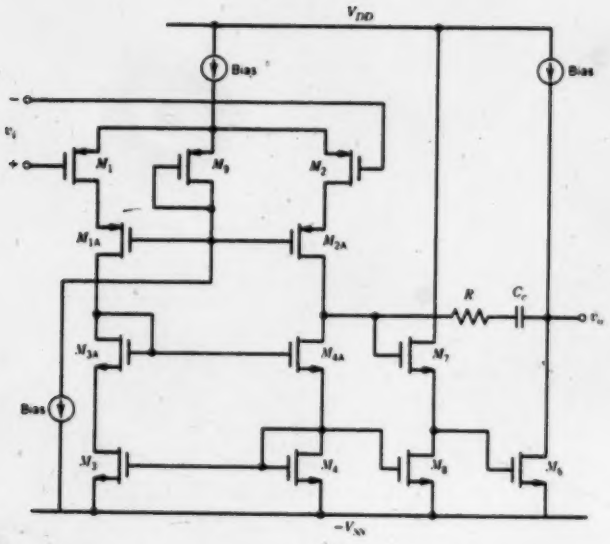


Figure 2.27 Op amp with cascoded first stage

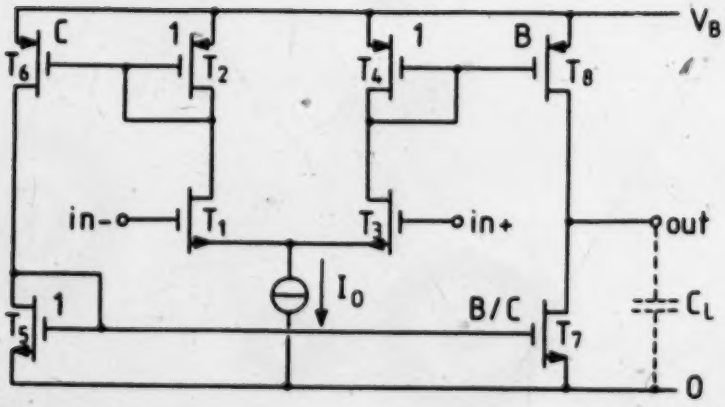


Figure 2.28 Operational transconductance amp

2.5.2 Single stage OAs

The high output impedance of the cascode configuration permits the gain of the regular 2-stage to be achieved in a single gain stage. The operational transconductance amplifer (OTA) of figure 2.28 is an example of such a single stage architecture [7]. Here the load capacitance provides the dominant pole for compensation and no Miller compensation capacitor is required. As such there is no right hand plane zero to degrade the phase margin. Also, the nondominant pole is set by small parasitic capacitors associated with the current mirrors instead of the large load capacitance as in the 2-stage design. The result is improved phase margin and better power efficiency (i.e. higher bandwidths achievable for same current). Also, because no Miller capacitor is used, the PSRR is improved (see section 2.2.7).

One disadvantage of the cascoded output is, as previously mentioned, the reduced output swing for which special biasing circuits are required. Also, because the entire gain of the amplifier is only achieved in the final portion of the circuit, more transistors will contribute noise to give a higher equivalent input noise. Finally the output impedance of the cascode output is very high which may be a problem in some applications. The folded cascode or common-source/common-gate amplifier of figure 2.29 [2] is another example of a single stage architecture.

2.5.3 Architectures for low power applications

The low power architectures seek to get around the problem of reduced slew rate when operating at low currents. Class AB circuitry such as in the second stage in figure 2.30 can be used to source or

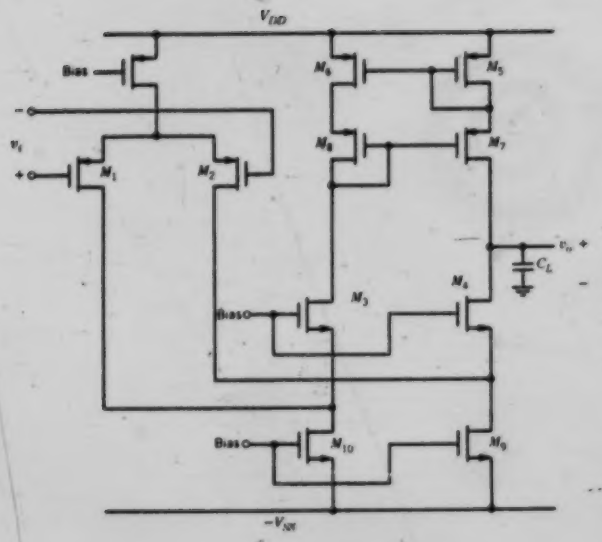


Figure 2.29 Folded cascode amp

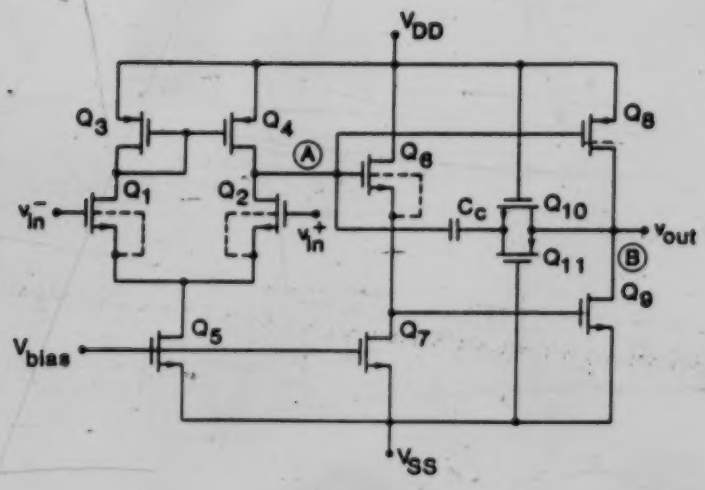


Figure 2.30 Circuit illustrating class AB second stage

sink higher currents than the DC quiescent values [2]. M2 is arranged as a driver in a push-pull arrangement instead of the simple current source of a regular two stage design. Another technique meant for switched capacitor applications uses a pulsed bias current source [8]. At the beginning of the clock phase the current is very high allowing rapid slewing of the outputs to close to their final value. By the end of the clock phase when no slewing is required, the current has diminished to a very low value. In [9] an adaptive biasing technique for the OTA is described whereby the bias current is made signal dependent. The result is a 100X improvement in slew rate (SR = 10V/μs for Ibias = 1 μA, C_L = 10 pF).

2.5.4 Circuit techniques for reducing offset and noise

The MOS transistor's ability to implement a switch has allowed the use of sampled data techniques to reduce offset to levels less than 1 mV with drift less than 2 μV/C and noise to levels of 65 nV/$\sqrt{\text{Hz}}$ at low frequencies [10].

Autozeroing or correlated double sampling [10] is a technique in which amplifer noise and offset are stored on capacitors during one clock phase. During the next phase the capacitors are switched into the signal path such that the stored voltage counters the noise and offset in the signal. Because of the high correlation of the low frequency noise in the two phases significant noise cancellation results. Switch change injection, clock feedthrough and thermal noise of switches then set the lower limit on achievable offset and noise.

One problem with autozeroing is that fast settling is required in order that the amplifier output can rapidly switch between the high

signal level and low offset level of subsequent phases. Chopper stabilization [11] is a technique which avoids this problem. The signal is square wave modulated before being amplified. When the output signal is demodulated the low frequency noise and offset of the amplifier are shifted outside the baseband of the signal and hence can be removed.

In both [10] and [11] the noise and offset reduction techniques are combined with fully differential circuitry. The dynamic range is thus further improved by allowing larger output swings. Also PSRR is improved since power supply variations produce a common mode signal on the differential output of one stage which is then rejected by the differential input of the next.

3.0 INTERNAL COMPENSATION TECHNIQUES

The purpose of this chapter is to investigate the optimum design and achievable performance for several compensation methods used in internal CMOS op amps. The methods presented are:

1) the use of a simple Miller capacitor;

2) the use of a resistor in series with the capacitor;

3) the use of a buffer in series with the capacitor; and

4) the use of a separate compensation stage.

Methods 2 and 3 are presented in the literature [4,5] as techniques which overcome the degraded phase margin due to signal feedforward in the Miller capacitor configuration. Method 4 is a new technique presented by this author. It will be seen that the achievable performance of the op amp in terms of power dissipation, die area, and settling time is dependent on the compensation method used.

3.1 General Considerations

3.1.1 Second Order System Model

The second order system approximation gives us a basis for understanding and comparing the different compensation techniques. Here the OA open loop frequency response is assumed to be as shown in figure 3.1 i.e. an integrator response with a single nondominant pole at $p > w_u$. The corresponding open loop transfer function would be:

$$A_{OL}(s) = \frac{w_u}{s} \frac{1}{1 + s/p} \qquad (3.1)$$

or normalizing with respect to w_u:

$$A_{OL}(s) = \frac{1}{s} \frac{1}{(1 + s/p')} = \frac{p'}{s\,(s + p')} \tag{3.2}$$

where $p' = p/w_u$.

With 100% feedback, the closed loop transfer function is then:

$$A_{CL}(s) = \frac{A_{OL}(s)}{1 + A_{OL}(s)} = \frac{p'}{s^2 + p's + p'} \tag{3.3}$$

The closed loop pole locations are then at:

$$s_{1,2} = -\frac{p'}{2} \left[1 \pm \sqrt{1 - 4/p'}\right] \tag{3.4}$$

The root locus plot of figure 3.2 shows these closed loop pole locations as a function of the open loop pole p'.

Knowing the closed loop pole locations, the inverse Laplace transform can be used to derive the time response to an input step. Figure 3.3 shows examples of the step response for different values of the open loop pole. Note that for $p'>4$ the system is overdamped and shows an exponential response.

An important fact in the compensation design is that the phase margin (in the open loop frequency response) is directly related to the value of p' and so can be used to predict the time response. From (3.2) the phase margin can be derived as:

$$PM = \tan^{-1} \sqrt{\frac{2}{\sqrt{1 + 4/p'^2} - 1}} \tag{3.5}$$

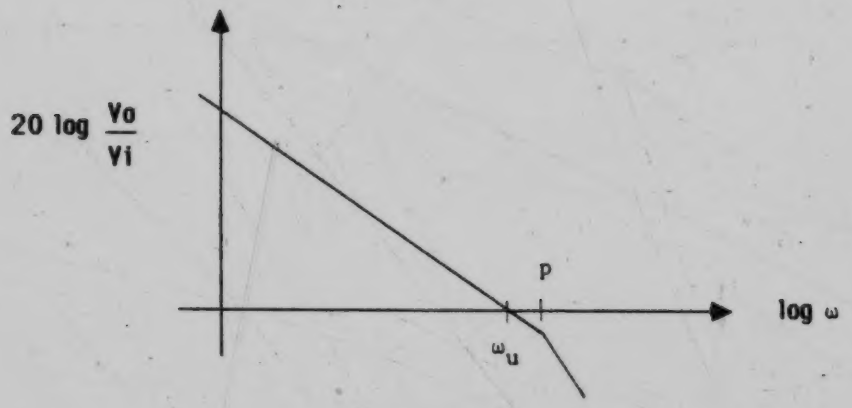


Figure 3.1 Simplified OA open loop frequency response

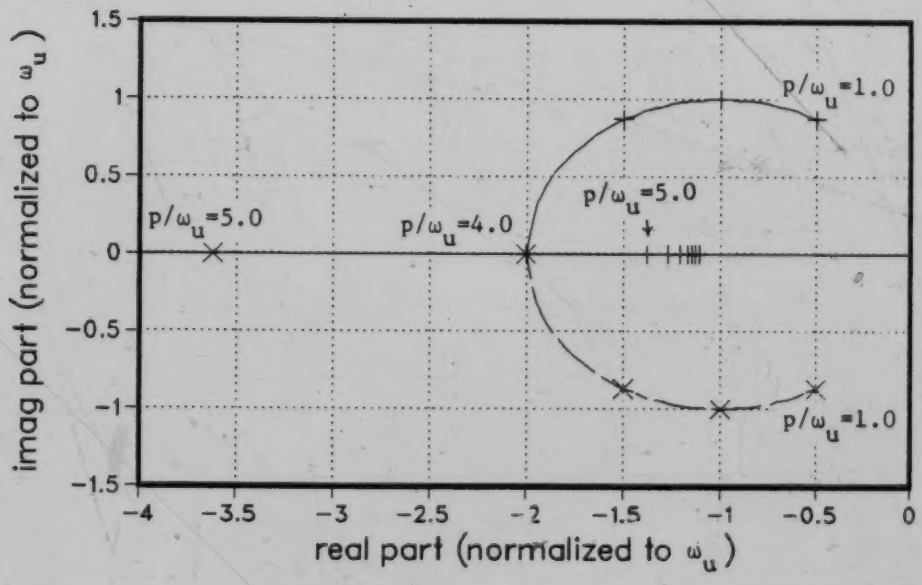


Figure 3.2 Root locus for 2nd order system

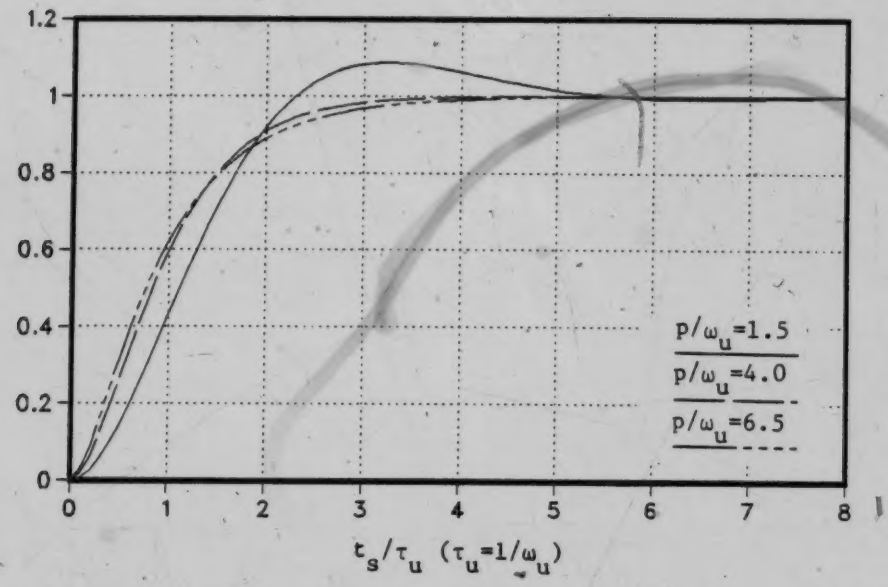


Figure 3.3 Step response for 2nd order system

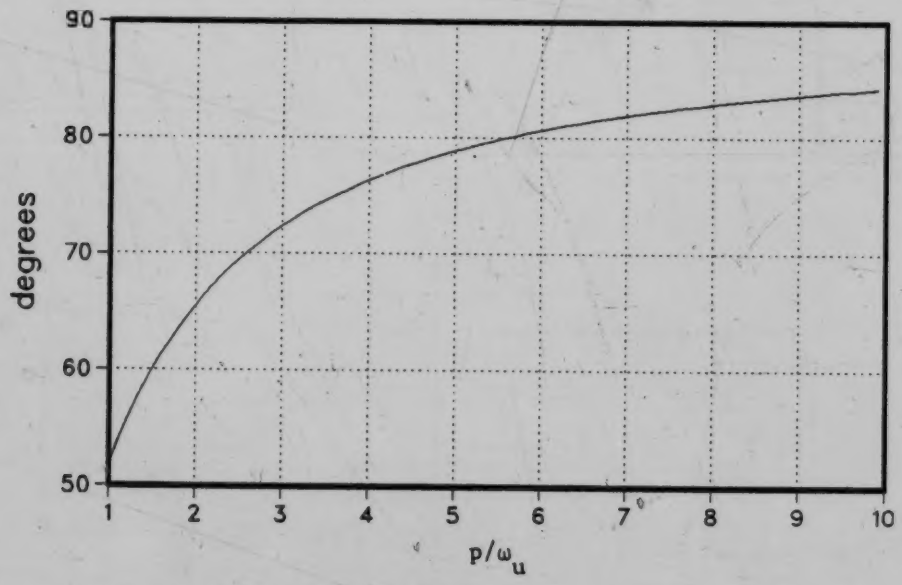


Figure 3.4 Phase margin vs open loop pole location for 2nd order system

Figure 3.4 shows the PM vs p'. Note that p'=1.5 corresponds to PM=60° which is the PM typically chosen for the classical two-stage OA design.

The settling time and overshoot of the step response are the design parameters of most interest here. For the second order system these can be easily derived and are shown in figures 3.5 and 3.6 as functions of the open loop pole location. Note that the minimum achievable settling time occurs at p'=3.35 where the overshoot is equal to the error band of 0.1%.

From figure 3.4, p'=3.35 corresponds to a phase margin of 74°. The usual 60° phase margin corresponds with p'=1.5 and results in an overshoot of 8.8% and t_s=8.35 τ_u which is about 2.4 X greater than the minimum. It will be shown that using the compensation techniques of this chapter the minimum settling can be more closely achieved with possible area and power savings as well.

3.1.2 Validity of second order assumption

An actual op amp does not have the open loop frequency response of figure 3.1. Parasitics in the first stage introduce higher order poles and zeros and the different compensation techniques also introduce additional poles and zeros. The question then arises as to when the results of the second order system analysis can be applied. It can be stated [15] that the correspondence between the phase margin and the step response will still hold if there is a dominant pair of complex conjugate closed loop poles and there are no zeros nearby. Hence high frequency poles and zeros can be taken into account in the second order model by deriving an equivalent single pole which gives the same phase margin as the actual multi pole/zero system.

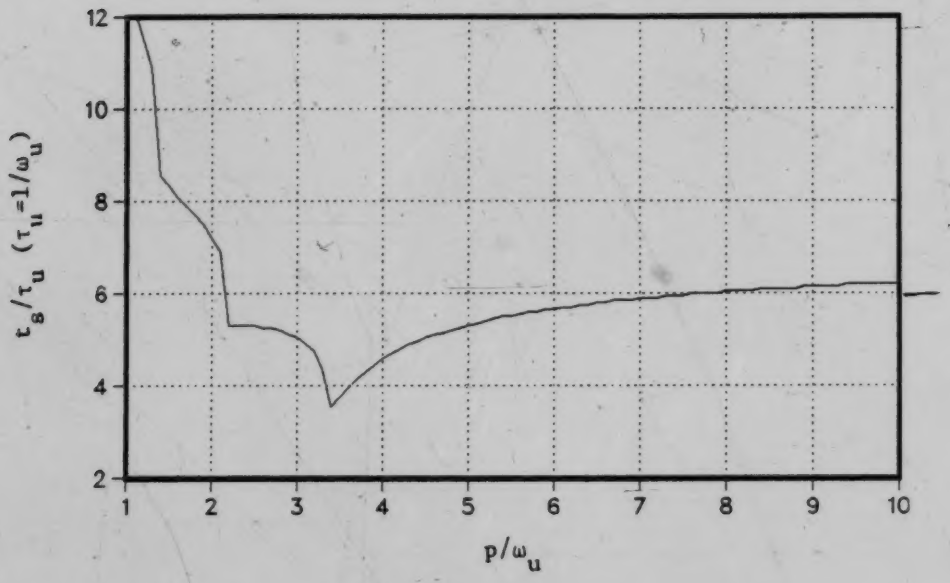


Figure 3.5 0.1% settling time for 2nd order system

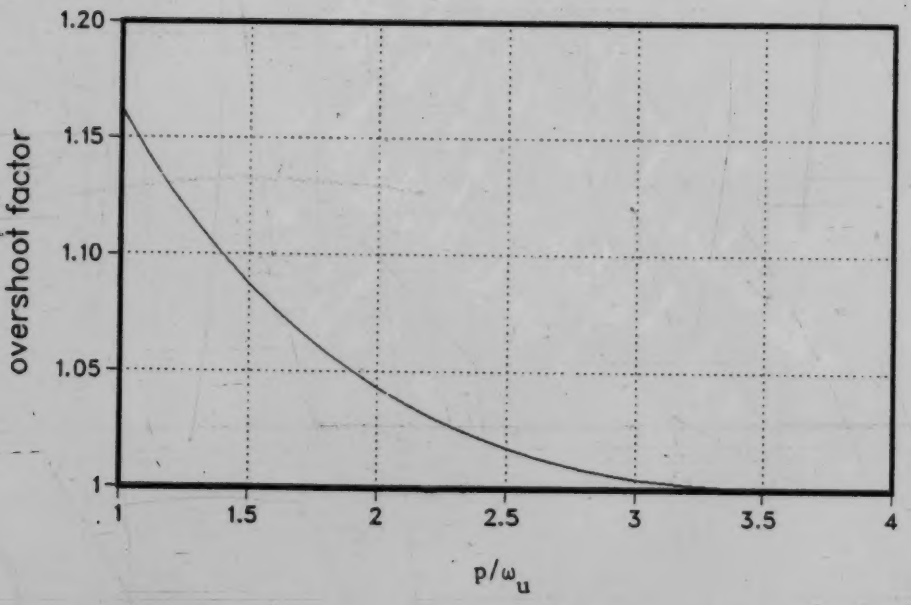


Figure 3.6 Overshoot for 2nd order system

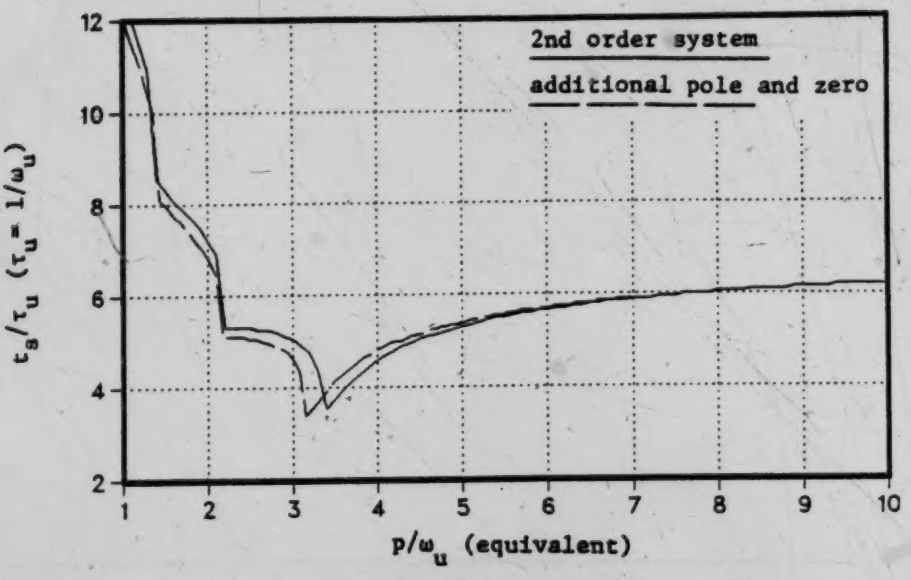
To get some idea of the accuracy of this approximation, an additional pole and zero at 10 and 20X w_u respectively were added to the open loop transfer function of (3.2). The settling time and overshoot were calculated and are plotted against the equivalent pole location in figure 3.7. Curves for the regular second order system are also included. The deviation between the two sets of curves is then the error of the approximation.

In the next sections it will be seen that the compensation techniques described often introduce closely spaced pole-zero pairs ("doublets"). If these doublets occur at frequencies near or below the unity-gain frequency there can be a significant effect on the settling time. The second order system results are then no longer directly valid but can be used for purposes of comparison.

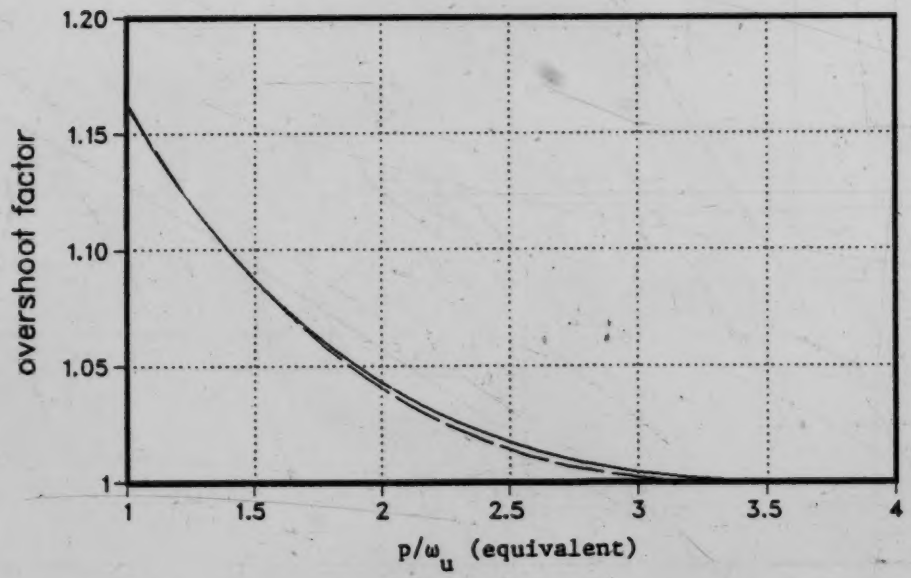
3.2 Series Buffer Compensation

3.2.1 Description

The simple Miller capacitor method of compensation suffers from a degraded phase margin due to the parallel path to the output which the capacitor presents to the signal at high frequencies (see section 2.2.3). This can be corrected by the use of a buffer in series with the capacitor as shown in figure 3.8(a). The buffer would be implemented using a source follower configuration. The implications to the OA performance would be a reduced output swing due to the gate-source voltage required to maintain the bias current of the source follower. Also, bias current will contribute to the overall power dissipation. However, it will be shown that this method can achieve



(a)

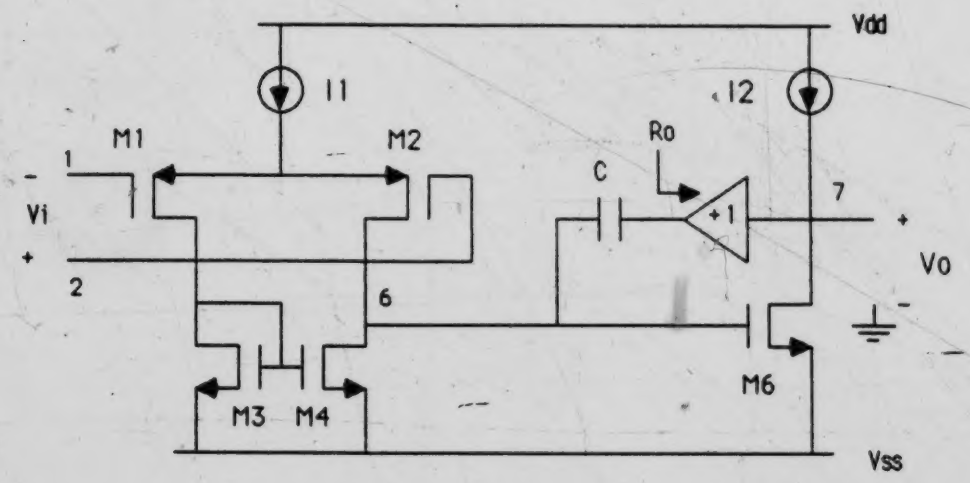


(b)

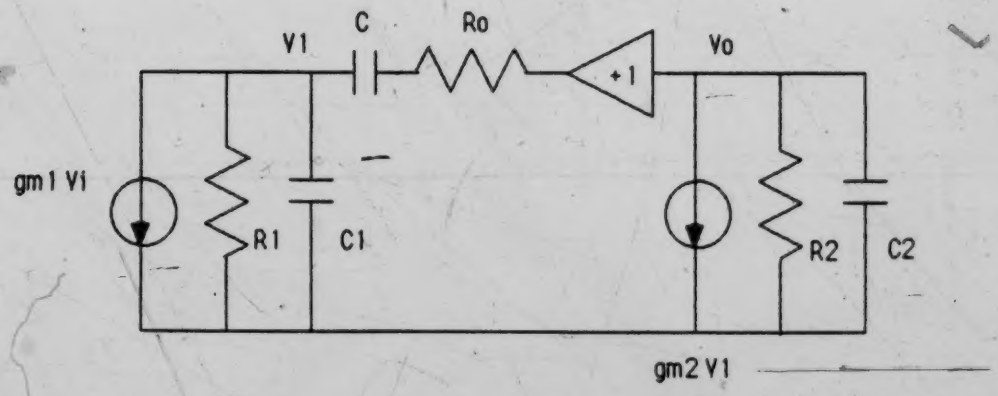
Figure 3.7 Accuracy of 2nd order assumption with pole and zero at 10 and 20 Mhz

(a) 0.1% settling time

(b) % overshoot



(a)



(b)

Figure 3.8 Compensation with a series buffer

(a) circuit

(b) small signal model

better compensation with lower overall power dissipation than the simple Miller capacitor method.

A linear analysis of the circuit can be made in order to show the expected performance under this assumption. It will be shown later, however, that nonlinearities have a strong effect on the resulting performance.

The small signal model of figure 3.8(b) is used to derive the following transfer function:

$$\frac{v_o}{v_i} \simeq g_{m1}g_{m2}R_1R_2 \frac{(1 + sRoC)}{(1 + sg_{m2}R_1R_2C)(1 + sC_2/g_{m2})(1 + sRoC_1)} \qquad (3.6)$$

Comparing this with the transfer function for the simple Miller capacitor shows that the right hand plane zero at g_{m2}/C is no longer present. Instead a left hand plane zero at $1/RoC$ and an additional hi-frequency pole at $1/RoC_1$ have been introduced.

3.2.2 Choosing Ro

In the design of the compensation, the question arises as to how Ro should be chosen. One approach might be to minimize Ro in order to minimize the effect of the extra pole. For example, by the use of a large aspect ratio and bias current the g_m of the source follower buffer is made equal to the g_m of the second stage. Then it is safe to say that the pole contributed by the buffer is insignificant since

$$p = \frac{1}{RoC_1} = \frac{g_{m2}}{C_1} \gg \frac{g_{m1}}{C} \qquad (g_{m2} > g_{m1},\ C_1 \ll C)$$

i.e. $p \gg w_u$

The LHP zero will then be located at

$$z = \frac{1}{RoC} = \frac{g_{m2}}{C} = \frac{10g_{m1}}{C} = 10w_u$$

if $g_{m2}=10\ g_{m1}$. The results of the second order system analysis can be used with the effect of the zero being an improvement of the phase margin by about $\tan^{-1}(1/10) \simeq 6^o$. Including the elimination of the RHP zero there would be a net phase margin improvement of 12^o over the simple Miller capacitor method.

However, even though there is improvement in phase margin, this approach is not optimum. If the same increase in bias current and die area were applied to the second stage with simple Miller compensation the phase margin is also improved without the extra devices and reduced output swing. If the second stage bias current were doubled, for instance, the phase margin improvement can be calculated to be about 14^o.

A better choice for Ro in terms of power efficiency is to take:

$$Ro = \frac{1}{g_{m2}} \frac{C_2}{C} \tag{3.7}$$

From (3.6) it is seen that the LHP zero then cancels the pole at g_{m2}/C_2 and the remaining nondominant pole is at

$$p = \frac{g_{m2}}{C_2} \frac{C}{C_1} \tag{3.8}$$

The new nondominant pole is thus seen to be increased in frequency by a factor of C/C_1 i.e. the ratio of the large compensation capacitor to a small parasitic. Hence now g_{m2} and second stage bias current I_2 can be reduced. Also, from (3.7) the source follower transconductance is lower than g_{m2} by a factor of C_2/C. Hence the power dissipation in the buffer is also reduced.

3.2.3 Power dissipation

Slew rate requirements limit the reduction of I_{tot} and g_{m2}. To prevent the first, second or buffer stages from limiting the SR requires:

$$\frac{I_1}{C} \geq SR, \quad \frac{I_{buffer}}{C} \geq SR, \quad \frac{I_2}{C_2} \geq SR \tag{3.9}$$

From (3.9) a lower limit on the total bias current can be written:

$$I_{tot} \geq SR\ (2C + C_2) \tag{3.10}$$

The design methods of this section result in $C \ll C_2$ hence (3.10) can be rewritten:

$$I_{tot} \geq SR\ C_2 \tag{3.11}$$

For the conventional design with $p_2 \geq 3w_u$ to give a phase margin of 60^o, the total bias current was found to be (see section 2.4.2, item 9):

$$I_{tot} \approx 3\ SR\ C_L\ (g_{m1}/g_{m6} + 1)$$

This suggests that about a factor of 3 improvement in power dissipation should be achievable using the series buffer compensation.

3.2.4 Lower limit on g_{m2}

From (3.9), a lower limit on g_{m2} can also be found:

$$\begin{aligned} \frac{I_2}{C_2} &\geq \frac{I_1}{C} \\ \frac{I_2}{I_1} &\geq \frac{C_2}{C} \\ \frac{I_2}{2I_3} &\geq \frac{C_2}{C} \\ \frac{g_{m2}}{2g_{m3}} &\geq \frac{C_2}{C} \end{aligned} \tag{3.12}$$

Now, since in a normal design $g_{m1}=K(2g_{m3})$ where $K\geq 1$ (see section 2.2.9). (3.12) can be rewritten:

$$\frac{g_{m2}}{g_{m1}} \geq \frac{1}{K}\frac{C_2}{C} \tag{3.13}$$

$$\frac{g_{m2}}{C_2} \geq \frac{1}{K}\frac{g_{m1}}{C} = \frac{w_u}{K} \tag{3.14}$$

For K=1, the lower limit on g_{m2} is then:

$$g_{m2}=w_u C_2 \tag{3.15}$$

This is still a factor of 3 X less than in the design using simple Miller capacitor compensation (see section 2.2.3). Note as well from (3.6) that this lower limit on g_{m2} results in a pole-zero pair at $g_{m2}/C_2=w_u$.

3.2.5 Choosing C

The compensation capacitor C is used to select the position of the nondominant pole p relative to w_u. Assuming C_1 is predominantly due to the gate capacitance of M6 (figure 3.8) (3.8) can be written:

$$p = \frac{g_{m2}}{C_1}\frac{C}{C_2} = \frac{g_{m3}}{C_3}\frac{C}{C_2} \tag{3.16}$$

(Here $L_2=L_3$ and $C_3=C_{ox}W_3L_3$). Hence the nondominant pole location is independent of the second stage (under bias conditions) and rather depends on the current mirror load (M3 and M4). The p/w_u ratio can then be written:

$$\frac{p}{w_u} = \frac{\frac{g_{m3}}{C_3}\frac{C}{C_2}}{\frac{g_{m1}}{C}} = \frac{g_{m3}}{g_{m1}}\frac{C^2}{C_3C_2} = \frac{C^2}{2KC_3C_2} \tag{3.17}$$

From (3.17) then, C can be chosen for a desired p/w_u ratio assuming values for the first stage parameters $K = \frac{g_{m1}}{2g_{m3}}$ and $C_3 = C_{ox}W_3L_3$.

Higher frequency poles and zeros due to the first stage contribute additional phase shift in the circuit. The effect of this is to push the effective value of p/w_u to a lower frequency than expected. In order to account for this, C must be increased until the phase margin corresponding to the desired value of p/w_u is obtained.

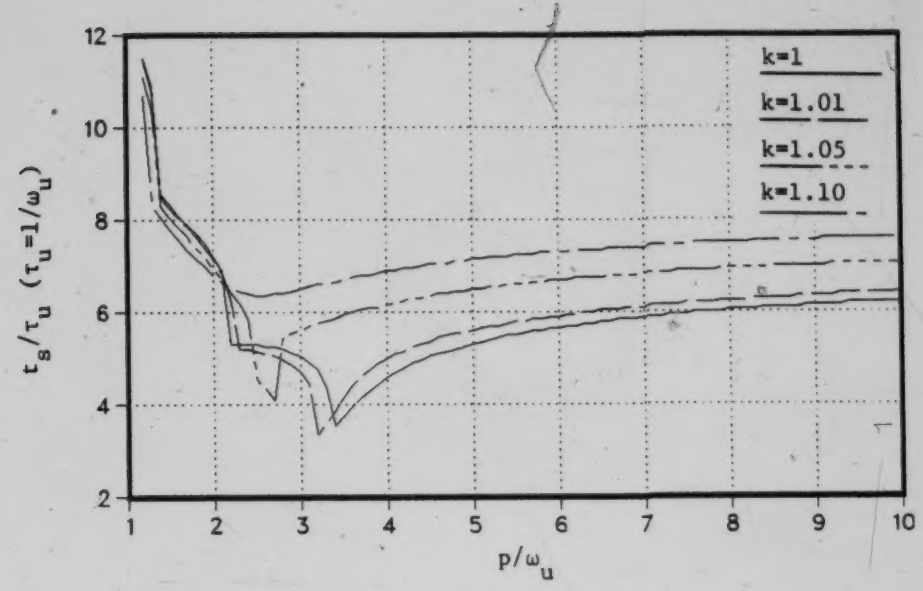
3.2.6 Factors affecting the step response

There are two factors which result in the fact that the step response differs from the results expected from the graphs of figures 3.5 and 3.6. These are imprecise pole/zero cancellation and the strong nonlinearity of the second stage at low current.

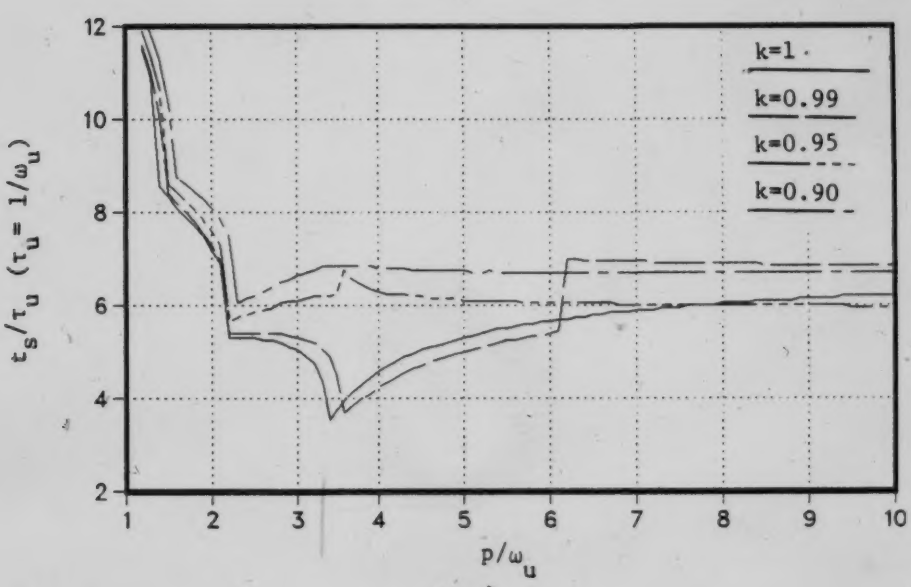
Imprecise pole/zero cancellation

The pole and zero at g_m/C_2 will not perfectly cancel each other for several reasons, namely: the approximate nature of the derivation of (3.6), process parameter variations and imprecise knowledge of the capacitance parasitics. The result is a closely spaced pole/zero pair or "doublet" which is at approximately w_u if I_2 is reduced to its lowest limit. Depending on the degree of mismatch, the doublet can have a significant effect on the locations of the closed loop poles and can dominate the settling time.

If the second order system analysis is modified to include the doublet with its zero at w_u, the settling time plots of figure 3.9



(a)



(b)

Figure 3.9 0.1% settling times with doublet at Wu

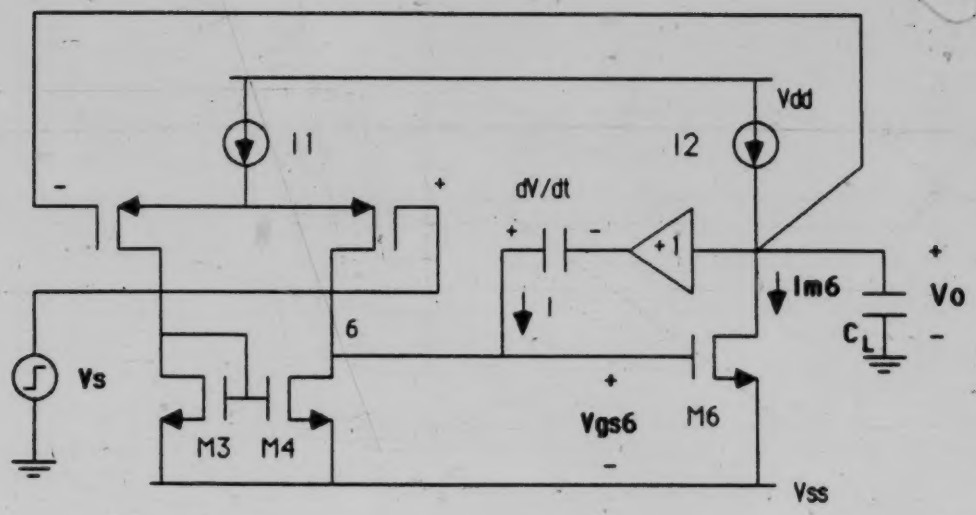
(a) k > 1
(b) k < 1

can be obtained. Each curve shows the 0.1% settling time (normalized to $\tau_u=1/w_u$) as a function of the nondominant pole location (normalized to w_u) for a different amount of pole/zero mismatch. This degree of mismatch is given by the matching parameter $k=p/z$ which is varied between 0.9 and 1.1. Curves for $k=1.0$ represent the simple second order system results and are included for comparison. From the curves it is seen that for mismatch greater than 2-3% the sharp minimum in the settling time observed for the simple second order system at $p/w_u=3.35$ is lost. However, with up to 10% mismatch, settling can be maintained below $t_s/\tau_u=7$ for $2.25 < p/w_u < 4.25$.

Nonlinear Second Stage

In the course of the step response, as the second stage driver current changes the transconductance can also change significantly. Hence, the nondominant pole of (3.8) and the doublet's pole location will change. It will be seen that for the minimum allowable value of I_2, this deviation of the poles is of such significance that the linear analysis cannot be used to accurately predict the step response.

The variation of second stage driver (M6) current during the response to a positive step input is shown in figure 3.10. The first stage draws current from the compensation capacitor resulting in a dV/dt across it. This gives the initial dip in the gate voltage of M6, causing its current to decrease and its active load current to be diverted to charge the load capacitance. As the rising dV/dt of the output comes to equal the dV/dt across the compensation capacitor, the gate voltage reaches the lowest point of its dip. The maximum deviation of the second stage bias current can then be derived as follows:



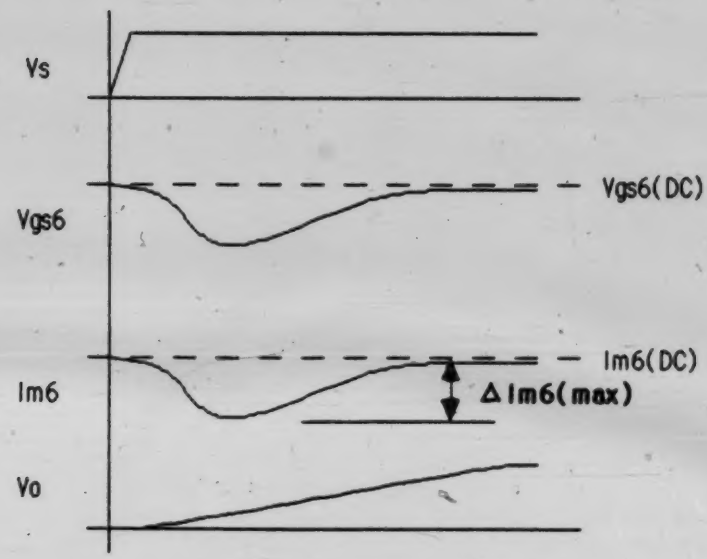


Figure 3.10 Waveforms for a positive step input

$$\frac{dV}{dt}_{out} = -\frac{dV}{dt}_{C} \tag{3.18}$$

$$\frac{I_2 - I_{M6(min)}}{C_L} = \frac{I}{C} \tag{3.19}$$

For $V_S < 1/2\ V_{DSAT1}$, $I = g_{m1}V_S$ as seen in the transfer function of the differential pair (figure 2.4). Hence,

$$\frac{\Delta I_{M6(max)}}{C_L} = -\frac{g_{m1}V_S}{C_L} \tag{3.20}$$

$$\Delta I_{M6(max)} = -(C_L\ w_u)\ V_S \tag{3.21}$$

For large V_S ($V_S \geq V_{DSAT}$), $I = I_1$ and so (3.21) is:

$$\Delta I_{M6(max)} = -C_L \frac{I_1}{C} = -(C_L\ SR) \tag{3.22}$$

Since the nondominant pole given by (3.8) and the doublet pole at g_{m2}/C_2 are both proportional to g_{m2}, the deviation of these pole locations is given by:

$$\frac{\Delta p}{p} = \frac{\Delta g_{m2}}{g_{m2}}$$

$$\frac{\Delta p}{p} = \frac{\sqrt{2(I_{M6} + \Delta I_{M6}\beta)} - \sqrt{2I_{M6}\beta}}{\sqrt{2I_{M6}\beta}}$$

$$\frac{\Delta p}{p} = \sqrt{1 + \frac{\Delta I_{M6}}{I_{M6}}} - 1 \tag{3.23}$$

From (3.22) and (3.23) the following results for large input steps can be calculated:

CASE	I_{M6}	$\Delta p/p$ +ve STEP	$\Delta p/p$ -ve STEP
1	SR C_L	-100%	+41%
2	1.25 (SR C_L)	- 55%	+34%
3	3 (SR C_L)	- 18%	+15%

Case #1 corresponds to a second stage current set at its lowest limit imposed by the slew rate. Case #2 corresponds to a value 25% higher than this lower limit. Case #3 corresponds to the high second stage bias level required in the conventional compensation scheme (see (2.28)).

From these results one sees that the pole deviation becomes quite large as second stage current is reduced to the slew rate limit. One can expect then that the linear analysis which assumes fixed pole locations can be highly inaccurate. For the PMOS input configuration, positive input steps result in a negative pole deviation. Hence the effective value of the nondominant pole p_2 is lower than expected resulting in undercompensation. Also, the doublet "splits" with the pole moving to a lower frequency resulting in some effective value of k lower than expected. (This also has an effect on the response as explained in the previous section). For negative input steps, the effective value of p_2 will be higher than expected (resulting in overcompensation) and the effective value of k will be higher than expected. For steps less than about $2V_{DSAT}$ the size of the step will determine the amount of pole deviation and hence the amount of over or undercompensation.

3.2.7 SPICE results

Simulations using SPICE (version 2G.6) were used to verify the above findings. Level 2 MOSFET models with Northern Telecom's 5 micron process parameters [2.3] were used. The series buffer compensation was designed with three different values of compensation capacitor: 2, 4.4 and 20 pF. The 2 pF and 4.4 pF designs were also repeated with the

high second stage current of conventional compensation. All the designs were derived from the conventional compensation design of figure 2.25. First stage device widths and currents were scaled by the same factor as the compensation capacitor so that the performance specs of table 2.3 (GBW, SR etc.) would not change. The series buffer and its output resistance were modelled using a voltage controlled voltage source and an ideal resistor. The value of Ro was chosen according to (3.7).

Table 3.1 summarizes the simulation results. Phase margins and the overshoot and settling times for positive and negative steps of up to 1 V are given. Results for the conventional compensation are in the first column for comparison. Phase margins were measured from the inverting input. A relative tolerance of 0.001% was chosen in the .OPTIONS statement for accurate transient response simulations. In order to better interpret the results, some of the doublet zero locations and mismatch factors are included. These were calculated from the exact transfer function of the small signal model of figure 3.9. Values for transconductances, and resistance and capacitance parasitics were taken from the SPICE operating point analysis.

In comparing the designs, those with low second stage current are seen to have overshoots and settling times dependent on the step size. Damping continuously decreases (i.e. more overshoot, longer settling) as the positive step size increases up until $V_S > 2V_{DSAT}$ (i.e. $V_S \approx .7$ V). For negative going steps, the damping increases (i.e. less overshoot). To compare with the expected results of the linear analysis, the 2 pF design has a phase margin of 76.5^o which corresponds to $p/w_u=4.1$, no overshoot and $t_S=0.75$ μs. (with

		CONVENTIONAL DESIGN		SERIES BUFFER, LOW CURRENT DESIGNS						SERIES BUFFER, HIGH CURRENT DESIGNS			
C		4.4 pF		2		4.4		20		2		4.4	
I2		120 μA		49.7		49.7		44		120		120	
g_{m2}		355 μA/V		155		148		132		373		355	
Ro		-		64516		31480		7576		26810		13444	
k		-		0.98						0.93			
z/w_u		-		1.27						3.1			
PM		60		76.5		82		84.5		76		81.5	
		Mp(%)	t_S(μs)	Mp	t_S	Mp	t_S	Mp	t_S	Mp	t_S	Mp	t_S
	1.0	4.3	1.65	2.2	1.58	1.0	1.5	1.35	1.66	0.7	1.7	-	1.04
	0.7	5.4	1.47	2.23	1.35	1.03	1.3	1.16	1.4				
	0.3	7.8	1.35	1.27	1.16	0.18	1.0	0.28	1.15	0.9	1.32	0.05	0.82
Step	0.1	7.8	1.31	0.45	1.1	0.02	0.85	0.05	0.84	0.8	1.32	0.04	0.81
	-0.1	7.5	1.27	0.3	1.14	-	0.96	-	0.97	0.9	1.41	0.02	0.80
	-0.3	6.8	1.25	0.12	1.08	-	1.025	-	1.05	0.9	1.45	0.04	0.795
	-0.7												
	-1.0	3.8	1.5	0.03	1.05	-	1.25	-	1.28	0.6	1.54	-	1.0

Table 3.1 Results of simulations on designs using series buffer compensation

k=0.98, figure 3.10 indicates t_s will be little altered). Even the 0.1 V step is seen to have higher overshoot and longer settling than expected. (One result which is not too clearly understood at the moment is why the high current design with 2 pF also has a substantially higher overshoot and settling than expected).

By increasing C and thereby pushing p/w_u out to higher frequency, the overshoot in the low current designs is seen to decrease up to a point. This can be explained as follows: as p/w_u moves out to higher frequency, the effect of its deviation becomes less significant and the splitting of the doublet at w_u becomes the predominant factor in affecting the step response. The effect of the p/w_u deviation seems negligible for phase margins greater than about 82° corresponding to $p/w_u \approx 7$. For the given designs this corresponded to $C/C_L \approx 1/4$. A similar improvement in overshoot and settling is seen in the high current designs.

In the 2 pF/low current design, it is seen that there are substantial power and area savings while maintaining or improving the settling and overshoot of the conventional design. However, the best step response is obtained when the same size compensation capacitor and same high second stage current are used.

3.3 Series Resistor Compensation

3.3.1 Description

Use of a series resistor as shown in figure 3.11(a) is another method which is used [4] to improve the simple Miller capacitor compensation. The resistor is implemented using a parallel P and N

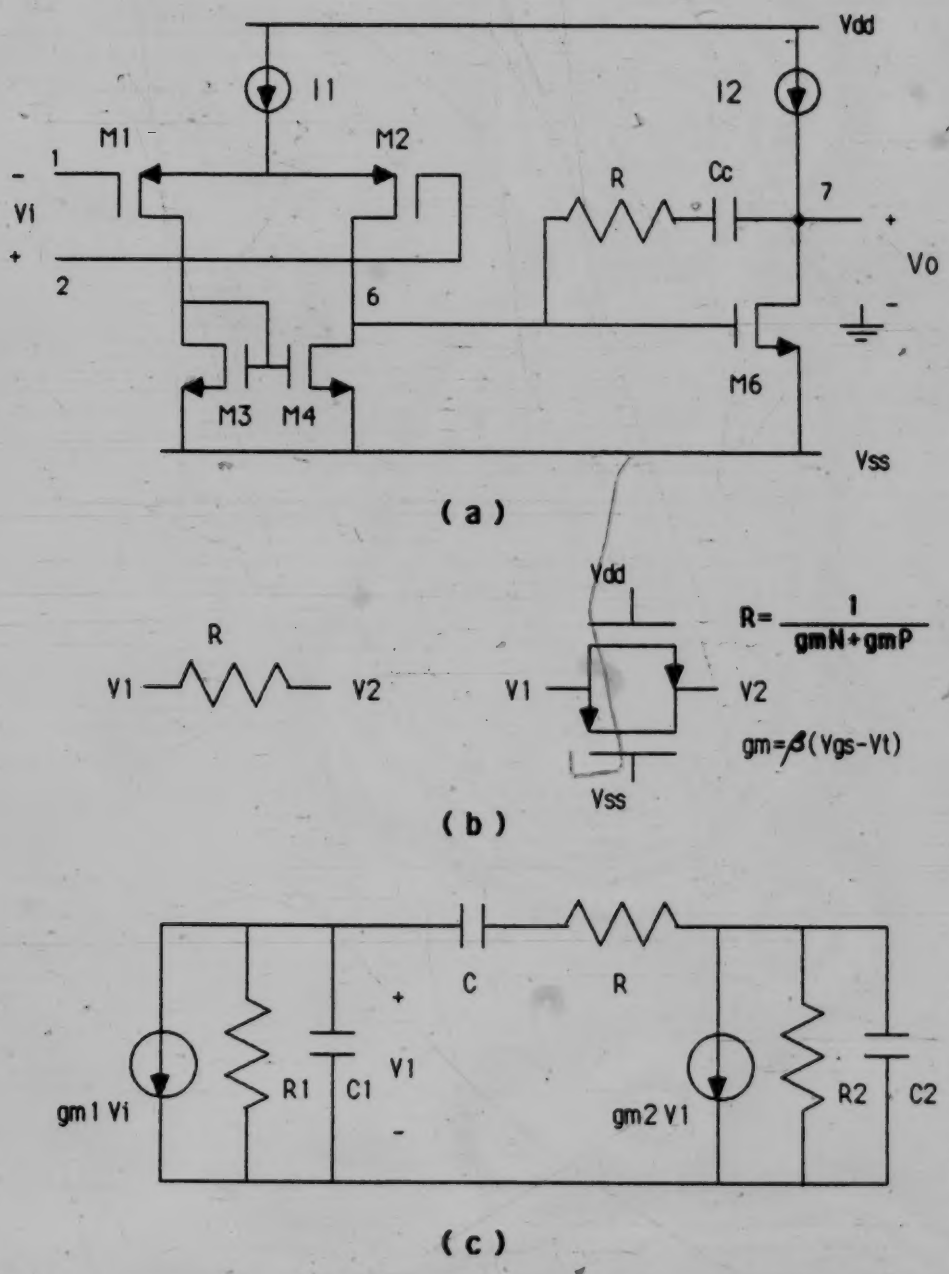


Figure 3.11 Compensation with a series resistor

(a) circuit
(b) resistor implementation
(c) small signal model

channel pass transistor as shown in figure 3.11(b). By implementing the pass transistors on the left side of the capacitor, the gate source voltages remain relatively fixed and the op amp output swing is not degraded.

The small signal model of figure 3.11(c) can be used to derive the following approximate transfer function:

$$\frac{v_o}{v_i} \simeq \frac{g_{m1}g_{m2}R_1R_2\ (1+s(R-1/g_{m2})C)\ (1+sRC)}{(1+sg_{m2}R_1R_2C)\ (1+sC_2/g_{m2})(1+sRC_1)(1+sRC)} \qquad (3.24)$$

The pole and zero at 1/RC are included to indicate what appears to be an imprecisely matched pole-zero pair here. However, exact calculations of the pole and zero locations for the designs given in section 3.3.6 seem to indicate that this pole-zero pair is matched to better than 0.05%. Hence it will be ignored in further discussion. Note that as in the case of compensation with the buffer, the series resistor also introduces an additional pole and zero. The zero exists in the right hand plane for $R < 1/g_{m2}$ and in the left hand plane for $R > 1/g_{m2}$.

3.3.2 Choosing R

From (3.24) it is seen that choosing $R=1/g_{m2}$ results in the cancellation of the right hand plane zero. The usual nondominant pole at g_{m2}/C_2 remains as well as an additional high frequency pole at g_{m2}/C_1. The net result is some improvement in the phase margin. The amount of this improvement depends on where the RHP zero was located. For $g_{m2}/g_{m1}=10$ the RHP zero is located at $10\ w_u$ (see 2.2.3) resulting in a phase margin improvement of about 5^o.

The resistor can also be chosen according to the same strategy of section 3.2 of using a LHP zero to cancel the main nondominant pole at g_{m2}/C_2. From (3.24) it is seen that selecting

$$R = \frac{1}{g_{m2}} \frac{C + C_2}{C} \tag{3.25}$$

results in a new nondominant pole at

$$p = \frac{g_{m2}}{C + C_2} \frac{C}{C_1} \tag{3.26}$$

and a doublet:

$$(p, z) = \frac{g_{m2}}{C_2} \tag{3.27}$$

Note the close similarity between these results and the results for the series buffer compensation as given in section 3.2.2. Here, though, the nondominant pole is at a slightly lower frequency because C_2 is replaced by $C + C_2$.

3.3.3 Slew rate limitations

As in the series buffer compensation, second stage current can be reduced up to a limit set by the SR. However, in this case the second stage must provide current for charging both C and C_2. The result is that even though there is no extra stage to bias, the lower limit on the total bias current is the same as given by (3.10) for the series buffer compensation. Also, the lower limit on g_{m2} can be found to be:

$$\frac{g_{m2}}{C_2} \geq K\left(1 + \frac{C}{C_2}\right)\frac{g_{m1}}{C} = w_u \tag{3.28}$$

where $K = \frac{g_{m1}}{2g_{m3}}$. The doublet will thus be again close to w_u.

3.3.4 Choosing C

The same derivation as used in section 3.2.5 can be used here with C_2 replaced by $C + C_2$. The result is that p/w_u is now given by:

$$\frac{p}{w_u} = \frac{K\,C_2}{2\,C_3(C_2 + C)} \tag{3.29}$$

from which C is found as

$$C = \frac{C_3}{K}\frac{p}{w_u}\left[1 + \sqrt{1 + 2K\frac{C_2}{C_3}\frac{w_u}{p}}\right] \tag{3.30}$$

Again the need to overcompensate to account for additional phase shifts applies here.

3.3.5 Factors affecting step response

Again as discussed in section 3.2.6, low second stage currents result in significant pole deviation during the course of the step response. Also, in view of the fact that the pole and doublet locations for the series resistor designs are very similar to those of the series buffer design, similar performance is expected here.

3.3.6 SPICE results

The results of SPICE simulations for two series resistor compensation designs are given in table 3.2. The same background information as given in section 3.2.7 applies here. Two of the designs are identical to two of the series buffer designs except that the buffer with its output resistance is replaced by a resistor of value given by (3.25). The remaining design is identical to the conventional compensation design except for the addition of $R=1/g_{m2}$ aimed at cancelling the RHP zero.

C	2 pF		4.4 pF		4.4 pF	
I2	49.7 μA		120 μA		120 μA	
g_{m2}	155 μA/V		355 μA/V		355 μA/V	
R	70968		15621		2817	
k	0.98					
z/w_u	1.25					
PM	75.6°		80°		64°	
Step	Mp(%)	t_s(μs)	Mp	t_s	Mp	t_s
1.0	3.2	1.58	-	0.96	3.0	1.55
0.7	3.3	1.37				
0.3	1.8	1.17	0.07	0.72	5.5	1.36
0.1	0.65	1.1	0.06	0.73	5.3	1.31
-0.1	0.35	1.13	0.06	0.735	5.2	1.24
-0.3	0.1	1.07	0.07	0.75	4.6	1.22
-0.7						
-1.0	0.03	1.07	-	0.96	2.3	1.16

Table 3.2 Simulation results for series resistor compensation designs

The first two designs show the same type of behaviour as in the series buffer designs. With the lower second stage current and the lower value of p/w_u, the damping of the step response shows a strong dependence on the step size for steps of up to $2V_{DSAT}$. For both these designs, however, the damping is slightly less than the corresponding series buffer designs. This is understandable since for the same value of compensation capacitor, (3.17) and (3.29) indicate that the series resistor design has a lower p/w_u value by a factor of $C/(C_2 + C)$. This effect is also seen in the lower phase margins.

The improved settling times of the high current design (with R given by (3.25)) relative to the series buffer case are explained in that the reduced damping brings the overshoot closer to the optimum of 0.1%.

As expected, the design in which $R=1/g_{m2}$ shows a small improvement in the phase margin (4^o) compared to the conventional compensation case (see table 3.1). As such there is only a small reduction in overshoot and settling time. Choosing $R=1/g_{m2}$ can be expected to give larger gains when g_{m1} is required to be larger for noise considerations. In this case, $g_{m2}/g_{m1} < 10$ and the RHP zero will move to lower frequency becoming more significant. Still, as seen in comparing the two 4.4 pF designs, choosing R according to (3.25) results in a much higher frequency nondominant pole and a superior response.

3.4 Separate Stage Compensation

A quite different approach to improving the conventional compensation is described in this section. The technique is simple and provides better phase margin for about the same power dissipation. A separate compensation stage matched to the output stage is used, resulting in a low-frequency pole-zero cancellation.

3.4.1 Small signal analysis

The proposed op amp is shown in figure 3.12 together with its small signal model. C_1, C_{pc} and C_{2p} represent parasitics. The subscript "c" refers to the compensation stage. A small signal analysis shows that at node 2 the transfer function is

$$\frac{v_2}{v_i} = g_{m1}R_1 \frac{(1+s/z)}{(1+s/p_1)(1+s/p_2)} \qquad (3.31)$$

where

$$z = \frac{1}{R_{2c}(C_{pc}+C_c)} \qquad (3.32)$$

$$p_1 = \frac{1}{g_{m2c}R_{2c}R_1C_c} \qquad (3.33)$$

$$p_2 \approx \frac{g_{m2c}}{C_1} \qquad (3.34)$$

The output node introduces an extra pole of value

$$p = \frac{1}{R_2(C_p+C_L)} \approx \frac{1}{R_2C_2} \qquad (3.35)$$

Now if the compensation stage is matched to the output stage and $C_C=C_L$ the output pole will cancel the zero of (3.32) to give an overall transfer function

$$\frac{v_o}{v_i} = -\frac{g_{m1}g_{m2}R_1R_2}{(1+s/p_1)(1+s/p_2)} \qquad (3.36)$$

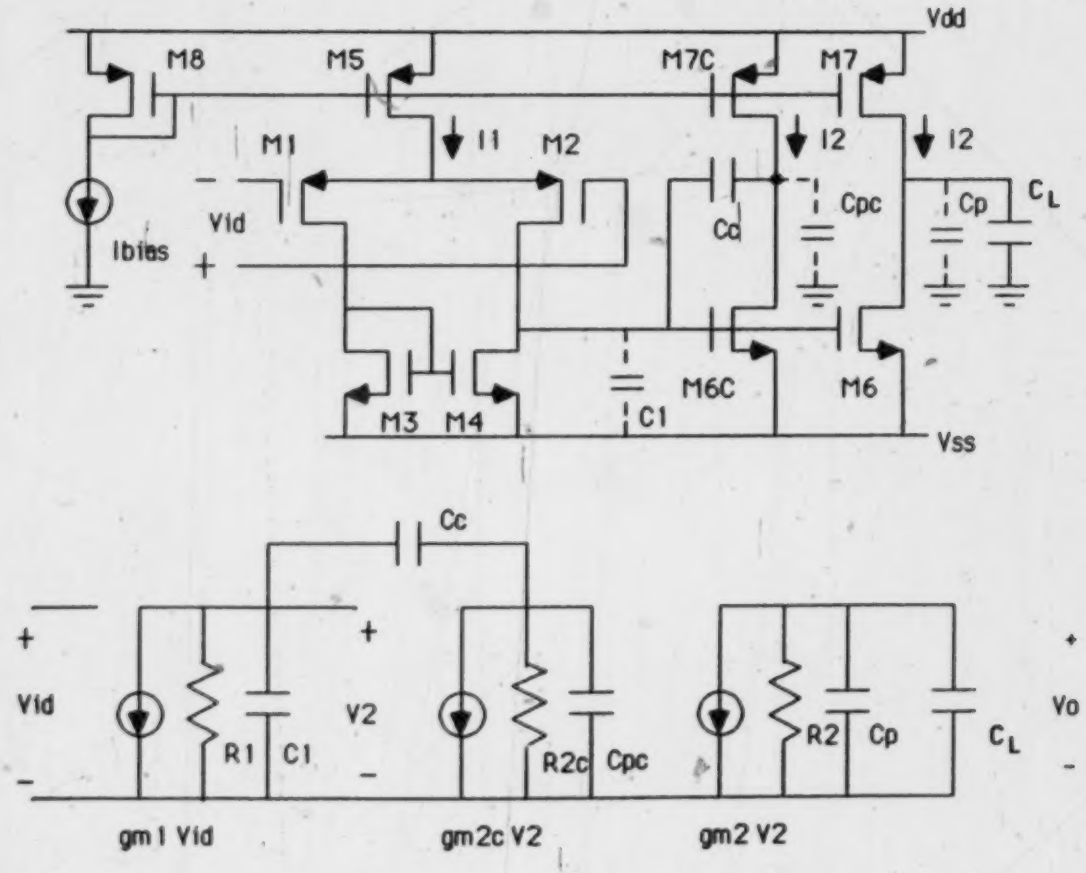


Figure 3.12 Separate stage compensation

3.4.2 Phase margin

For a given power dissipation the phase margin of the separate stage compensation design is greatly improved over the conventional design. From (3.31) we note that the right hand plane zero which normally degrades phase margin does not appear. The reason is that the compensation capacitor no longer provides a path for signals to propagate directly to the output at high frequencies. As well, now the nondominant pole p_2 is dependent on a small parasitic C_1 rather than a large load capacitance. This arises because the separate compensation stage is not loaded down by C_L. The result is that the nondominant pole will be further out in frequency and will have much less effect on the phase margin.

The nondominant pole location can be shown to be largely independent of the second stage conditions. Assuming C_1 is predominantly due to the gate capacitance of M6 and M6C (figure 3.15) gives the result:

$$p_2 = \frac{g_{m2}}{C_1} = \frac{g_{m3}}{2C_3} \tag{3.37}$$

thus p_2 is given by 1/2 x f_T of the first stage mirror load. Typically, the nondominant pole will be at more than an order of magnitude higher frequency than in the conventional design.

3.4.3 Power dissipation

The above points suggest that second stage bias current can be reduced for a given phase margin. However, slew rate requirements dictate that second stage current cannot be less than in the first stage. Furthermore, the first stage current must be increased to

account for the larger compensation capacitor. The lower limit for the bias current of each of the three stages is given by:

$$\frac{I_{bias}}{C_2} \geq SR$$

Thus the total bias current is:

$$I_{tot} \geq 3\ SR\ C_2 \tag{3.38}$$

Comparing this to (2.28) shows that the minimum power dissipation will be about the same as for the conventional compensation design with a phase margin of 60^o.

3.4.4 Settling time

Thus, though the power dissipation over the conventional design is not reduced, the phase margin can approach 90^o due to the much higher frequency nondominant pole. The closed loop system can then be described as a single pole system with an exponential step response and a settling time given by:

$$t_s = \tau_u \ln(1/\epsilon) \tag{3.39}$$

where $\pm\epsilon$ is the error band to which settling is measured and $\tau_u = 1/w_u$. For $\epsilon = 0.001$ (0.1% settling)

$$t_s = 6.9\ \tau_u \tag{3.40}$$

This is about a 20% improvement over the settling time for the conventional design with a phase margin of 60^o. However, as seen in the next section, this settling time may be degraded if the cancelling pole-zero pair at low frequency are not matched closely enough.

3.4.5 Matching requirements

Imperfect matching of the compensation stage with the output stage or C_C with C_L will result in imprecise pole/zero cancellation. The transfer function (3.31) will then contain a closely spaced pole-zero pair (termed a "doublet") which may have an imperceptible effect on the frequency response but can dramatically increase the closed loop settling time for small error bands.

It can be shown [12] that with a doublet the voltage follower step response is approximately given by

$$Vo(t) = V_S[a(1 - \exp\frac{-t}{\tau_u}) + b(1 - \exp\frac{-t}{\tau_z})] \qquad (3.41)$$

where $\tau_u = 1/w_u$ and $\tau_z = 1/w_z$ are time constants corresponding to the unity gain frequency and doublet frequency respectively. Also

$$a = 1 - \frac{k-1}{A_1-1} \text{ and } b = \frac{k-1}{A_1-1} \qquad (3.42)$$

where A_1 is the open loop gain at the doublet frequency and $k = w_p/w_z$ is the relative doublet separation. (Here slewing is ignored and the op amp is assumed to have no nondominant poles).

Relation (3.41) indicates a step response consisting of a main fast exponential which quickly brings the output to within a coarse error band and a slow exponential response for the remaining settling time. The slow settling component will not degrade the settling time if it falls completely within the desired error band. From (3.42) this requires

$$\frac{|k-1|}{A_1-1} < \epsilon \qquad (3.43)$$

For our case the gain at the doublet is

$$A_1 = Av(0)\,\frac{1/p_1}{1/z} = g_{m1}g_{m2}R_1R_2\,\frac{R_2C_C}{g_{m2}R_2R_1C_C} = g_{m1}R_2 \qquad (3.44)$$

where p_1 and z are given by (3.33) and (3.32). Thus A_1 can be expected to be about 50 and for ϵ=0.001 (0.1% settling) (3.43) indicates that the pole/zero mismatch must be kept to less than 5%.

3.4.6 Power supply rejection

The separate stage compensation also results in improved power supply rejection compared to the conventional design. We consider here the negative supply rejection ratio

$$-PSRR = \frac{v_o/v_{i(w)}}{v_o/vss(w)} \qquad (3.45)$$

Here v_o/v_i and v_o/vss are the transfer functions from the differential input and from the negative supply to the output, respectively. For the PMOS input configuration +PSRR (positive supply rejection ratio) is typically 20dB better than -PSRR [15] and so only the latter is used as a figure of merit.

Figure 3.13 shows the small signal model used to derive v_o/vss for the separate compensation stage op amp. (Here the number subscripts correspond to the transistors in figure 3.12). The result is

$$\frac{v_o}{vss} = \frac{R_7}{R_6+R_7}\;\frac{1+s/z}{1+s/p_1}\;\frac{1}{1+s/p_2} \qquad (3.46)$$

where

$$z = \frac{1}{(g_{m6}R_6)(R_2||R_4)C_C} \qquad (3.47)$$

$$p_1 = (1 + R_6/R_7)z \qquad (3.48)$$

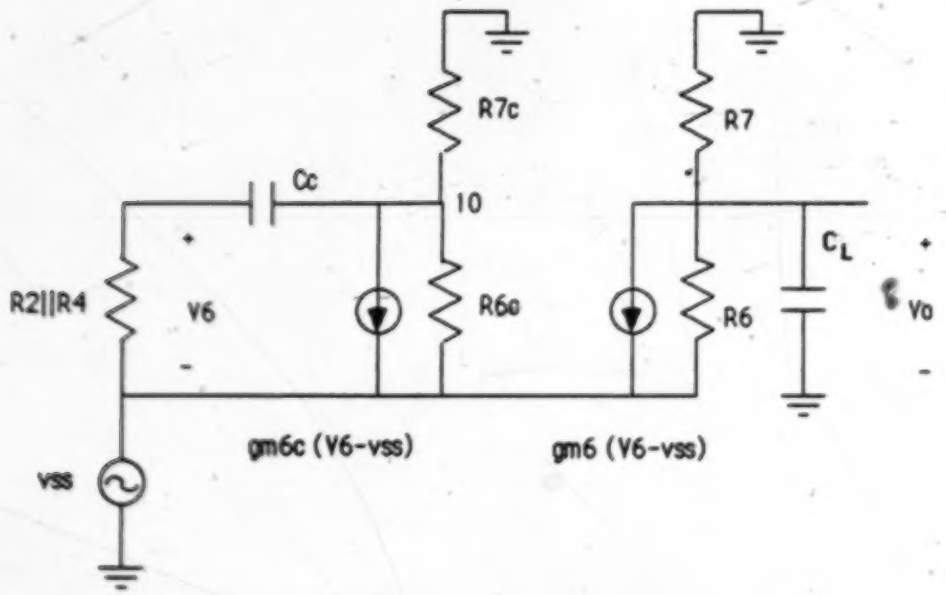


Figure 3.13 Model for calculating negative PSRR

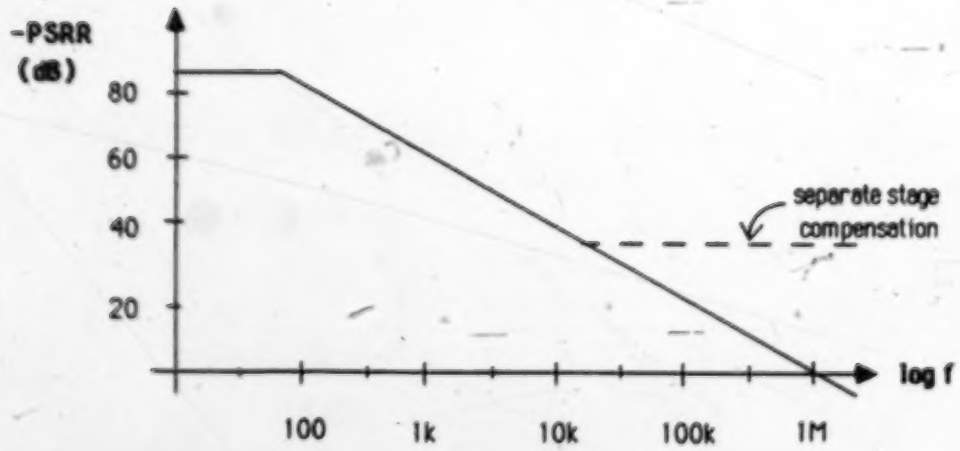


Figure 3.14 Negative PSRR for separate stage
and convensional compensation design

and

$$p_2 = \frac{1}{(R_6||R_7)C_L} \qquad (3.49)$$

The zero z and p_1 arise from the compensation capacitor appearing as a short as frequency increases. M6C in figure 3.12 then appears as a diode connected transistor and the gain from the negative supply to node 10 (compensation stage output) rises to approach unity. M6 mirrors the action resulting in the same behaviour at the output node.

The extra pole p_2 appears due to the load capacitor at the output node. It would not appear if the output node were not isolated from the compensation capacitor. Hence using a separate compensation stage allows extra attenuation in the supply signal path resulting in improved -PSRR at high frequencies.

3.4.7 SPICE results

SPICE simulation results for a separate stage compensation design together with a conventional compensation design are given in table 3.4 and figure 3.14. Both designs meet the performance specs of table 2.3 and so have the same GBW and SR (remaining background information is the same as in section 3.2.7). Table 3.3 gives the compensation component values, stage currents and transistor widths for the designs. All gate lengths were chosen to be 10 micron in order to get sufficient gain. Note that first stage currents and device sizes are simply scaled by the same factor as the compensation capacitor ratio.

The results confirm that for the same power dissipation, the separate stage compensation gives an improved step response with no overshoot and reduced settling. Note that unlike the series buffer and

	Conventional Compensation	Separate Stage Compensation
M1, M2	W = 78 μm	356 μm
M3, M4	10	45
M5, M8	64	289
M6, (M6c)	240	90
M7, (M7c)	768	289
I1	9.2 μA	40.8 μA
I2	119.0 μA	44.0 μA
Cc	4.4 pF	20 pF
C_L	20 pF	20 pF

Table 3.3 Separate stage and conventional compensation design circuit parameters

	Conventional Compensation	Separate Stage Compensation
PM	59.4°	83.2°
P_{diss}	1.28 mW	1.29 mW
GAIN (DC)	73.6 dB	73.7 dB
GBW	0.96 MHz	0.97 MHz
SR	1.9 V/μs	1.8 V/μs
+ICMR	V_{DD} -1.5 V	V_{DD} -1.5 V
-ICMR	V_{SS}	V_{SS}
Vo swing	within 0.5 V of supply	same
CMRR(DC)	82.4 dB	83 dB
(1 kHz)	60 dB	60 dB
-PSRR(DC)	82 dB	82 dB
(100 kHz)	20 dB	35 dB
+PSRR(DC)	105 dB	105 dB
(100 kHz)	58 dB	61 dB

Step	Mp(%)	t_s(μs)	Mp	t_s
1.0	4.3	1.65	-	1.3
0.7	5.4	1.47	-	1.18
0.3	7.8	1.35	-	1.1
0.1	7.8	1.31	-	1.075
-0.1	7.5	1.27	-	1.02
-0.3	6.8	1.25	-	1.0
-0.7			-	1.08
-1.0	3.8	1.5	-	1.2

Table 3.4 Comparison of simulation results for separate stage compensation and conventional compensation designs

resistor designs with low second stage current, here the step size shows little effect on the step response. Also, the step response corresponds much more closely with the expected results from the linear analysis. p/w_u=8.25 corresponds to the 85° phase margin. From the second order system analysis results of figure 3.5 this gives an exponential response with a settling time of 0.96 μs. The explanation to the above points is as follows. Because this configuration inherently uses a large compensation capacitor, the nondominant pole as given by (3.37) is at high frequency. In the case of this design, p_2 = 40 MHz. However, from the phase margin it is seen that additional phase shifts (speculated as being due to the first stage) are such that the effective value of p_2 is at about 8 MHz. This can be imagined as resulting from the pole at 40 MHz and another one at 10 MHz representing the additional phase shifts. Thus, even if p_2 were to see a deviation of -50%, there would be little deviation of the effective value which would drop from 8 MHz to 6.7 MHz. As such, the step size has little effect on the transient response. Although the above points also apply to the series buffer design with C=20 pF, in that case there was also a doublet at about w_u which split to an extent dependent on the step size. Hence for the series buffer design the transient response was still seen to be dependent on step size even when p_2 was at high frequency.

Another point to mention here is that the simulation results are for the case when the doublet at the location given by (3.35) is closely matched. For an actual circuit implementation additional mismatch can be expected due to process variations causing the output

resistances of the two stages to differ and due to imprecise knowledge of the load capacitance.

Figure 3.17 graphically compares the negative PSRR for the conventional and the separate stage compensations. As expected, the pole contributed by the output node allows -PSRR to stay flat at 35dB for frequencies above 10 kHz. These PSRR measurements were obtained using the circuit configuration of figure 2.8 and so are valid up to the unity gain frequency f_u.

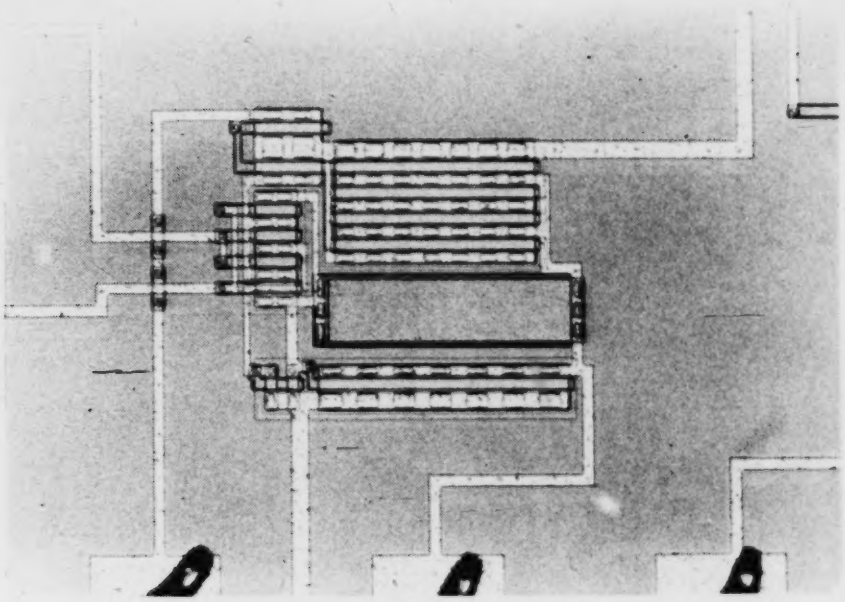
4.0 EXPERIMENTAL RESULTS

4.1 Op amp implementation

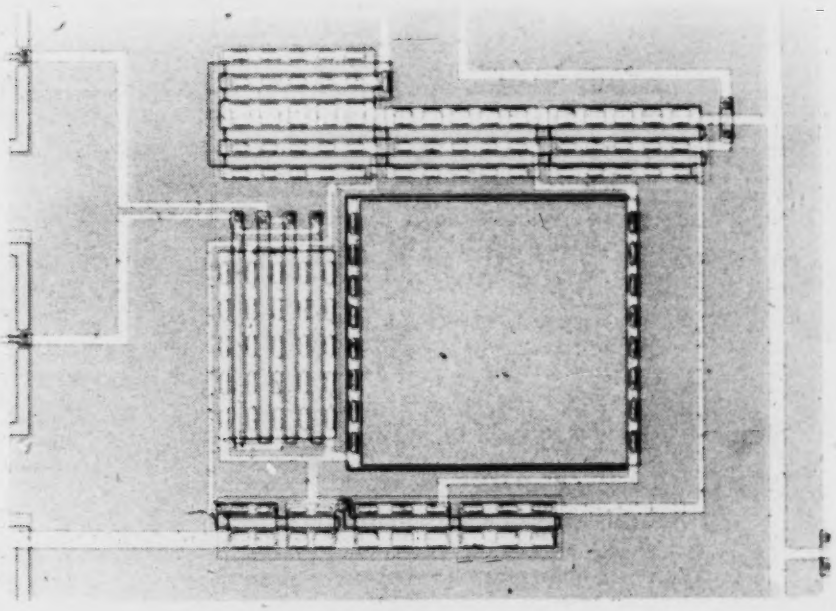
The conventional compensation and separate stage compensation designs given in table 3.3 were implemented in Northern Telecom's 5 micron process through the services of the Canadian Microelectronics Corporation [3]. Figure 4.1 shows photomicrographs of the implemented OA circuits. The conventional compensation design (OA1) takes up an area of about 94,000 square microns while the separate stage design takes up about twice this area mainly due to the larger compensation capacitor.

The circuit mask layers were generated on color graphics terminals using 'kic', the circuit layout program from Stanford University. For best matching, devices were kept as close together as possible and given the same orientation. Each transistor of the input pair was implemented using two parallel devices of half the width and the two sets of transistors were then arranged in a common centroid geometry [1]. In order to keep the circuit compact, very wide transistors were also implemented using smaller width devices connected in parallel. Protection circuits were used on the OA inputs. Bias currents for the OAs were set by external resistors.

Two sets of OAs were laid out, one set had all inputs and outputs going to pins while the other set were internally configured for unity gain and had the rated load capacitance and buffered outputs (see figure 4.2). This buffered version permitted step response



(a)



(b)

Figure 4.1 Photomicrographs of implemented OAs
(a) OA1 : conventional compensation
(b) OA2 : separate stage compensation

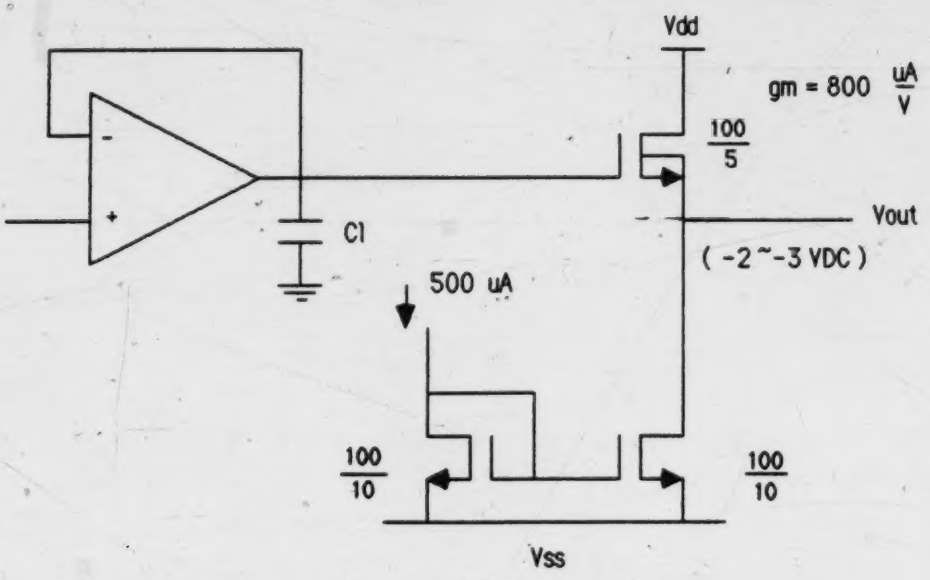


Figure 4.2 Buffered version of implemented OAs.

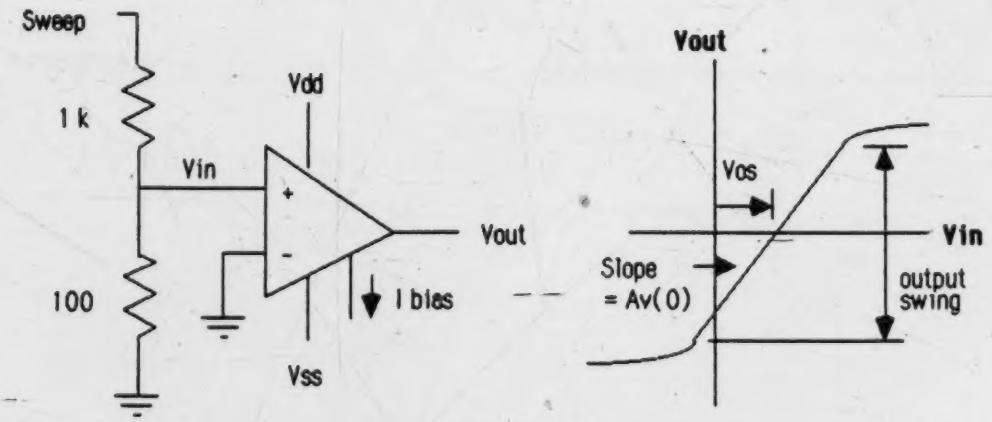


Figure 4.3 Open loop measurement on semiconductor parameter analyser

measurements to be made under the design conditions without having to worry about probe capacitance and parasitics.

The results of measurements on the OAs are given in tables 4.1 and 4.2 and in figure 4.12. The following sections explain how the measurements were undertaken.

4.2 Open loop DC measurements

Open loop DC transfer characteristics for the OAs were obtained on the HP4145A semiconductor parameter analyser. This allowed measuring the offset, DC gain and output swing as seen in figure 4.3. A resistive divider is used on the OA input in order to increase the resolution of the steps on the input sweep to less than 1 mV. Figure 4.4 shows a sample plot corresponding to OA2 chip #4. (The plot includes IDD as well as the open loop characteristic). The characteristic shows Av(0) ≈ 6000, Vos ≈ 3 mV and an output swing within about 0.7 V of the positive supply and 0.5 V of the negative supply. Note that noise causes irregularities over the 'linear' region of the curve. This is minimized by setting the parameter analyser on medium to long scale integration time. Regardless, the DC gain measurement is estimated as being accurate to within ± 20%.

4.3 Closed loop DC measurements

Closed loop DC transfer characteristics were also obtained on the parameter analyser. The OA is connected in a unity gain configuration and a staircase sweep is applied to the positive input through a source

CHIP #	1	2	3	4	5
Av(0)	6700	8000	6500	7200	7000
Vos (mV)	0	-12.4	-3.2	+0.3	+7.0
+OS (V)	V_{DD} -0.55	-0.6	-0.5	-0.6	-0.7
-OS (V)	V_{SS} +0.55	+0.5	+0.5	+0.5	+0.5
P_{diss} (mW)	1.28	1.31	1.31	1.38	1.35
+ICMR (V)	3.4	3.2	3.3	3.3	3.2
-ICMR (V)	-4.9	-4.9	-4.9	-4.9	-4.9
+PSRR(DC)	70.15 dB	65.2	76.04	100.1	80.12
CMRR(DC)	71.7 dB	65.4	81.1	81.6	73.7
SR (V/μs)					
rising	2	1.92	1.94	1.86	*
falling	2.2	2.12	2.15	2.02	
1 V step settling (μs)					
rising	1.52	1.58	1.52	1.60	*
falling	1.40	1.50	1.40	1.52	
f_u (MHz)	0.95				*
PM (degrees)	60				*

(* chip accidentally destroyed)

Table 4.1 OA1 measurement results

CHIP #	1	2	3	4	5
Av(0)	5700	6400	5400	6000	5500
Vos (mV)	-3.8	2.5	4.0	3.2	-14.7
+OS (V)	V_{DD} -0.6V	-0.7	-0.55	-0.65	-0.45
-OS (V)	V_{SS} +0.6V	+0.45	+0.55	+0.5	+0.45
P_{diss} (mW)	1.31	1.25	1.31	1.31	1.24
+ICMR (V)	3.2	3.2	3.2	3.2	3.1
-ICMR (V)	-4.9	-4.9	-4.9	-4.9	-4.9
+PSRR(DC)	100 dB	71.3	74.4	68.4	56.0
CMRR(DC)	82.7 dB	68.6	70.3	66.5	56.8
SR (V/μs)					
rising	1.72	1.68	1.6	1.61	*
falling	1.91	1.86	2.0	1.81	
rising 1 V step					
settling (μs)	2.5$^+$	1.19	10.9$^+$	1.15	*
overshoot (mV)	1.15	0.5	4.0	0.9	
falling 1 V step					
settling (μs)	1.1	1.17	12.1$^+$	1.15	*
overshoot (mV)	0.95	0.5	3.0	0.9	
f_u (MHz)	1.05	—			*
PM (degrees)	80				*

(* chip accidentally destroyed)
($^+$ effect of imprecise pole/zero cancellation)

Table 4.2 OA2 measurement results

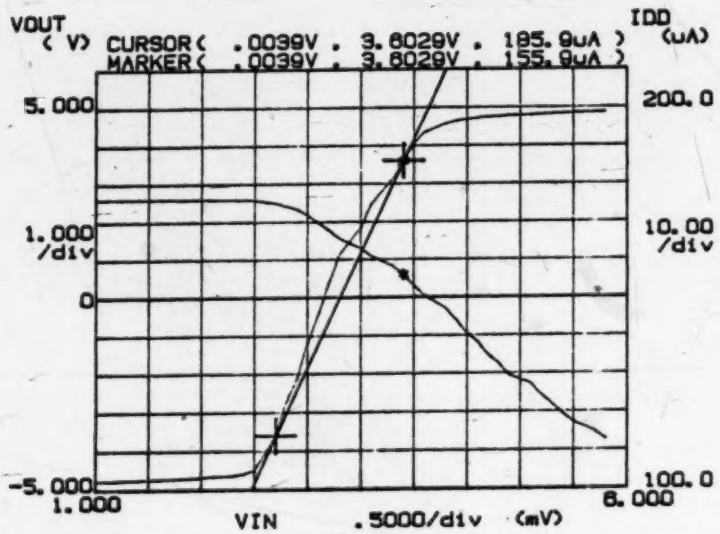


Figure 4.4 Open loop transfer characteristic

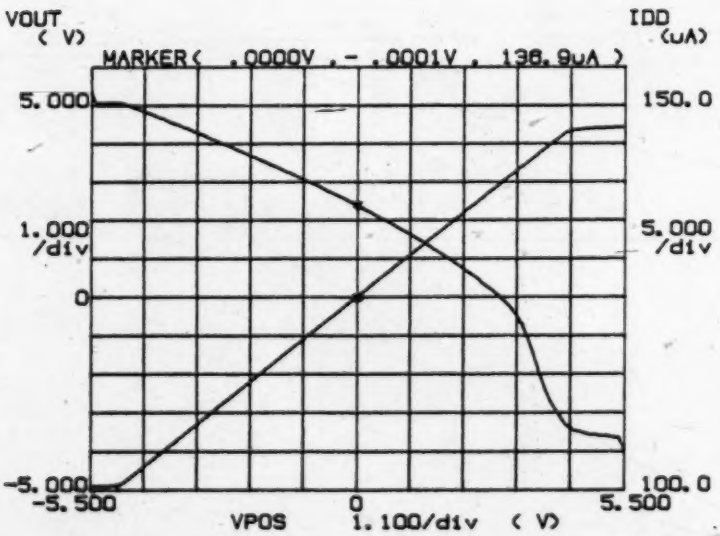


Figure 4.5 Closed loop transfer characteristic

channel. An LM356 op amp with ± 15 V supplies was used to buffer the output of the OA under test. If this was not done, the loading of the cabling and analyser input was observed to cause the OA to oscillate. Figure 4.5 shows the DC transfer characteristic for OA1 chip #1. Both I_{DD} and Vout are plotted. Three input ranges are observed: a negative range past which Vout levels off, a similar positive range and another reduced positive range past which I_{DD} drops off. This last range would correspond to the expected +ICMR past which M5 (figure 2.1) leaves pinchoff. It is speculated that the reason the transfer characteristic still appears linear past this point is that as first stage current drops, the resulting increase in gain counteracts the increasing offset due to mismatch of the second stage. Regardless of the linear characteristic, the SR can be expected to be reduced for inputs exceeding the +ICMR. The reason why I_{DD} levels off after dropping is not fully understood. As seen in the plot and on all the measured OAs, the -ICMR was seen to extend to -4.9 V. Although the -ICMR of the input stage was expected to extend to close to or including V_{SS}, it was expected that the limited output swing of the second stage would have caused the transfer characteristic to level off at about -4.5 V.

4.4 Slew rate measurements

To isolate the probe and any parasitic capacitances and to ensure a known load capacitance the buffered version of the OAs were used. The slew rate was measured for a 3 V input step. Figure 4.6 shows a picture of the 3 V step response for OA1.

4.5 Settling time measurements

The buffered OAs were used to measure the 0.1% settling for a 1 V step input. Figure 4.7 shows the 1 V step response for the two designs. Note that OA1 shows an overshoot of about 4% as expected (see table 3.4) while OA2 shows no overshoot. The spikes on the waveforms are due to the capacitive parasitics of the breadboard allowing the pulse input on adjacent pins to couple into the OA outputs.

The breadboarded circuit of figure 4.8 was used to make the settling time measurements. The circuit was derived from [12]. The spike waveform of figure 4.9 is seen at the center of the resistive divider as the output of the device under test (DUT) cancels the output of the hi-speed inverting amp. Since the DUT is slower, its settling corresponds with the settling of the spike. Because the spike waveform has no DC content its settling can be observed using AC coupling on the most sensitive scale of the oscilloscope. To ensure this is the case, the 10k pot is used to account for the unequal gains of the DUT and the inverting amp. Note that the spike amplitude is sufficiently small to prevent an excessive scope overload recovery time [12]. The high frequency N channel JFET is used to isolate the scope input capacitance. The LM318 inverting amp is configured for fast settling (see data sheets) and is made to have a negative output offset approximately equal to the DC level shift of the DUT's internal buffer. In this way none of the bias current meant for the buffer is redirected through the resistive divider.

Figure 4.10 shows the center spike of figure 4.9 on the most sensitive scale. The waveform shows OA1's 0.1% settling time for a 1 V

Figure 4.6 3V step response of OA1

Figure 4.7 1V step response
(Lower and upper traces correspond to OA1 and OA2 respectively)

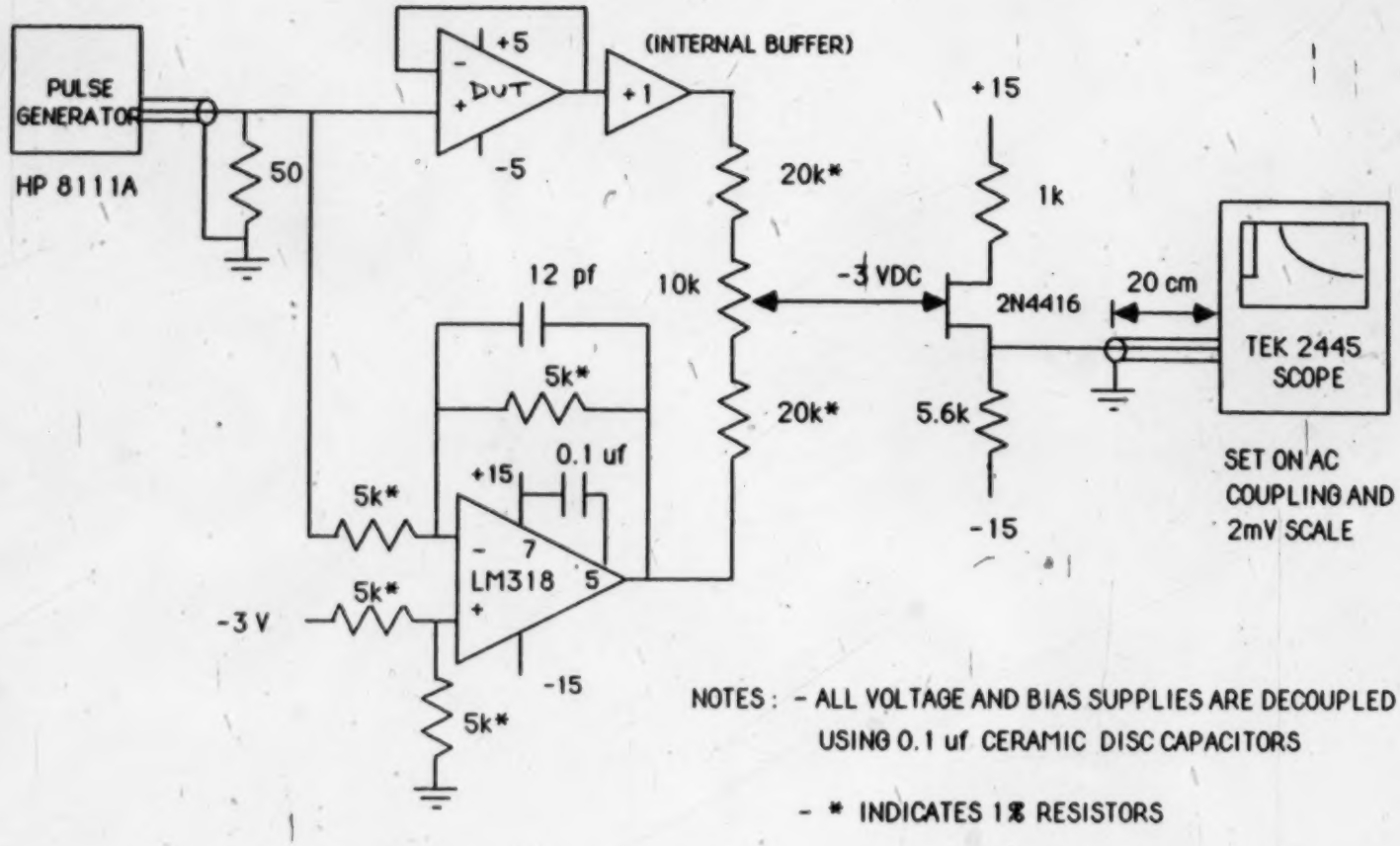


Figure 4.8 Circuit used to make settling time measurement

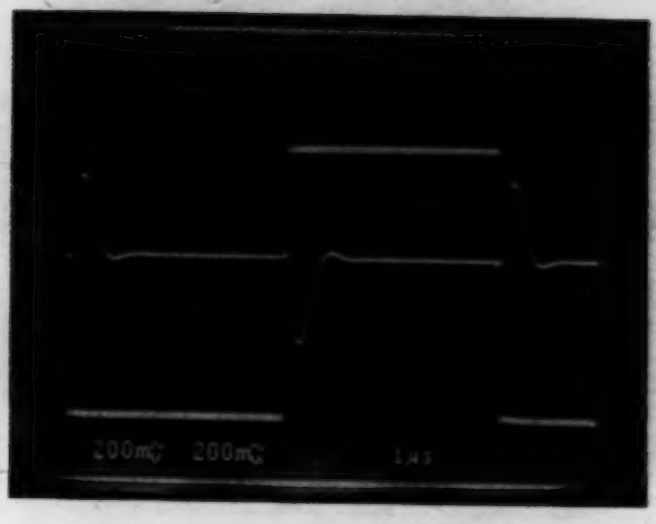


Figure 4.9 Input pulse and spike waveforms seen at center of divider in settling circuit

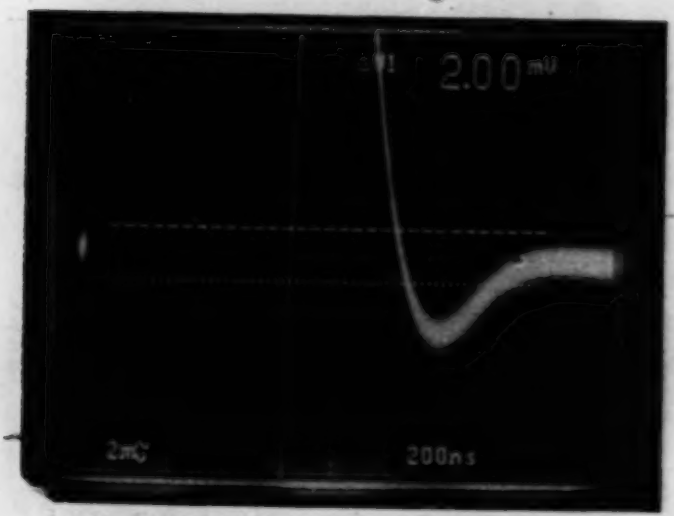


Figure 4.10 Middle spike of fig. 4.9 as seen on most sensitive scale

rising step. The white spot on the left side of the photo corresponds to the start of the pulse and the settling time is measured to where the trace settles within the ± 1 mV error band. The settling time of the test circuit itself was measured to be 0.69 μs by replacing the DUT by a wire link. Hence it is sufficiently less so as not to interfere with the settling of the DUT.

4.6 Phase margin and unity gain frequency

For the frequency response measurements the unbuffered OA was connected in a unity gain inverting configuration. 100 kohm resistors were selected as a tradeoff between a large value for minimum loading of the OA and a small value so that parasitics have least effect on the circuit. The total load capacitance on the OA was not accurately known but was estimated to be about 20 pF since a TEK P6131 probe was used (10.8 pF) and on the breadboard the pins adjacent to the output pin were at AC ground (~ 6 pF). A 200 mV peak signal at 1 MHz was applied to the input of the inverting amp configuration. An oscilloscope was used to monitor the waveforms on the output and inverting input of the OA. At the unity gain frequency the two waveforms are of equal amplitude. The phase difference is then measured on the oscilloscope.

4.7 Negative PSRR measurement

Figure 4.11 shows the circuit configuration used. The negative PSRR is given [12] by:

$$-PSRR\ (f) = \frac{vss(f)}{v_o\ (f)} \left[1 + \frac{R2}{R1}\right] \qquad (4.1)$$

R2 and R1 are chosen as 1m and 10k respectively and are measured on a multimeter for increased accuracy of the calculation. For measurements above 4 kHz the resistors are removed and the OA configured for unity gain. If this was not done the results were in error presumably due to the effects of parasitics in the breadboarded circuit. The AC signal on V_{SS} was chosen as 2 V peak to peak and is taken from an HP8111A function generator. The results of the measurements are given in figure 4.12.

4.8 Positive PSRR and CMRR measurement

Figure 4.11 shows the circuit configuration. The DC rejection ratio is given by:

$$+PSRR(DC) = \frac{\Delta V_{DD}}{\Delta Vo}\left(1 + \frac{R2}{R1}\right) \qquad (4.2)$$

ΔV_{DD} = 2 V was chosen. The bias resistor was connected to the negative side of the V_{DD} supply to ensure a constant bias current regardless of the shift applied to V_{DD}.

Figure 4.13 shows the circuit configuration for the CMRR measurement. The CMRR is given [12] by:

$$CMRR(DC) = \frac{\Delta Vcm}{\Delta Vdmm}\left(1 + \frac{R2}{R1}\right) \qquad (4.3)$$

where here ΔVcm = 4 V was used. The additional OA in the CMRR measurement circuit is required to increase the differential mode gain and so reduce an error component in the output signal which is due to the finiteness of this gain. Because this OA must be highly overcompensated for total loop stability, only the DC CMRR is measured.

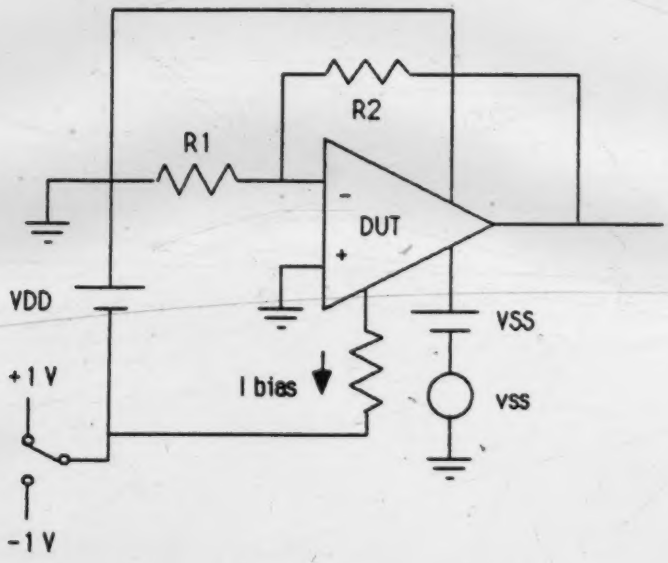


Figure 4.11 Configuration for measuring PSRR

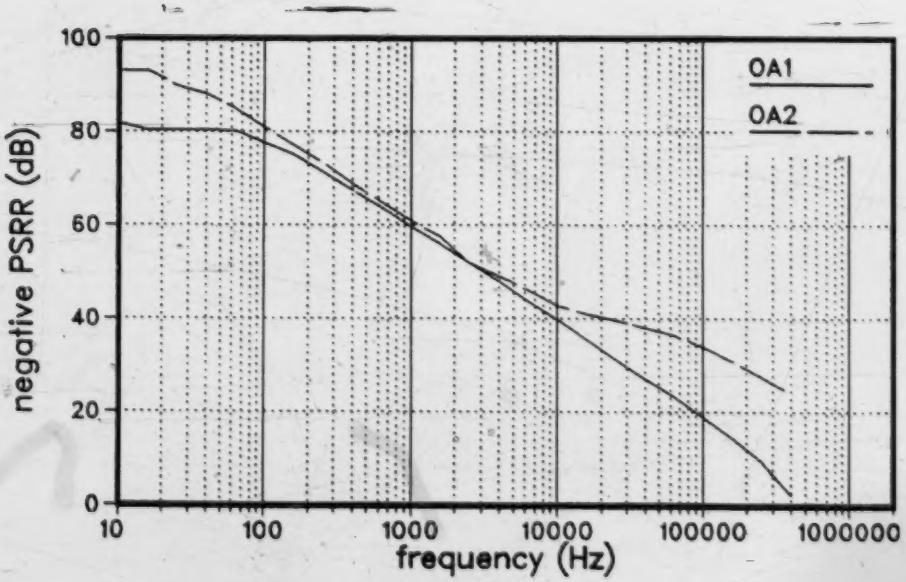


Figure 4.12 Negative PSRR

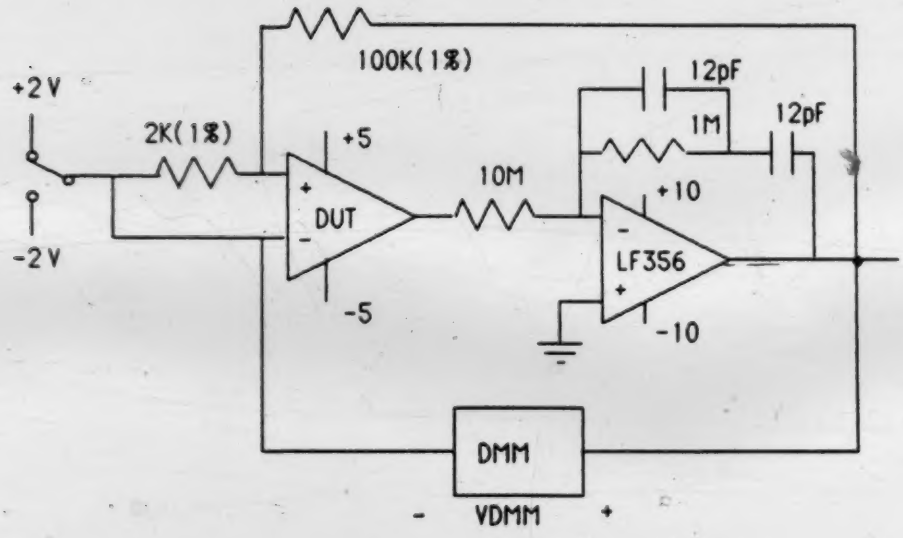


Figure 4.13 Configuration for measuring CMRR

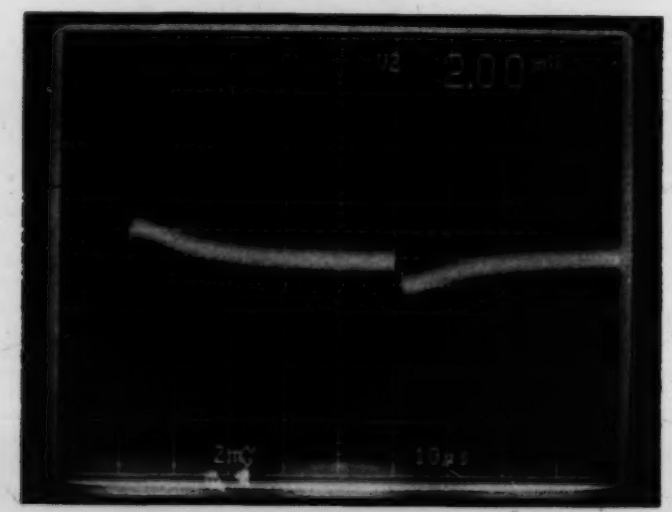


Figure 4.14 OA2 settling time waveform showing 'long tail' due to pole-zero mismatch.

4.9 Discussion of Results

The experimental results can be compared with the SPICE results listed in table 3.4. From the viewpoint of the previous chapter's discussion on compensation, the most relevant measurements are the phase margin and settling times. The phase margins are seen to be as expected for a 20 pF load although the actual load capacitance in the measurement circuit was not accurately known. However, both OAs can be expected to have had the same loading conditions and hence the difference in the phase margins is then the more valid result. As expected, the separate stage compensation design is seen to have about a 20 degree improvement in phase margin over the conventional design. This fact is also revealed in the lack of ringing in OA2's step response as seen in figure 4.7. The settling times for OA1 are about as expected. For all the samples of OA2 the step response showed an overshoot and the 'long tail' which is evidence of a pole/zero mismatch [12] (see figure 4.4). For 2 of the 4 measurements the overshoot remained within the error band and hence the settling time was not degraded. For these cases the OA2 settling time was about 20% faster than for OA1 as expected. However, for the cases where the overshoot exceeded the error band the settling was seriously degraded (chip #3 shows a 10X increase!) Some of the mismatch can be explained by the fact that the output stage drives a different capacitive load than the compensation stage. The output stage drives both the OA inverting input and a buffer input which represent about 1 pF. This is already 5% of the total load capacitance. From (3.32) and (3.35) then it is seen that the pole will be at about 5% lower frequency than the zero.

As explained in 3.4.5 the overshoot can thus be expected to be about on the same level as the error band. The spread in the overshoot for the 4 chips is attributed to process tolerances.

The improvement in the higher frequency -PSRR of OA2 over OA1 is observed in the results of figure 4.12. As expected the -PSRR of OA2 begins to level off near 35 dB for frequencies above about 20 kHz whereas OA1 continues to fall.

In the other performance areas, the two OAs are roughly equal. Both of the OA gains are higher than the expected gain of about 4900. The average gain for OA1 is about 7000 while that of OA2 is 5800. Both gains show about ± 10% variation over the 5 chips although how much of this variation may be due to the inaccuracy of the measurement is not known. Power dissipation is about as expected with roughly 6% variation. The +ICMR on all the samples is about 10% less than expected and the output swing on several of the chips does not meet the specification. This suggests that the OAs should be designed with a 10% margin on the +ICMR and as much as a 40% margin on the output swing to account for the process variations. Slew rates are within 15% of the expected 2 V/μs. Rising slew rates can be expected to be less than design values due to the parasitic capacitance at the sources of the input pair (see [13]).

Offset voltages, CMRR(DC) and +PSRR(DC) all show wide variation over the 5 chips. The worst offset was 15 mV while the best offsets were less than 0.5 mV. The best CMRR and +PSRR measurements corresponded with the expected results from the SPICE simulations although the worst values were as low as 56 dB. The reason for this is that the SPICE simulations assumed perfectly matched devices in the

first stage whereas mismatches in the implemented circuit have a strong effect on the CMRR. A mismatch of as little as 1% in the transconductance of the input transistors can result in the CMRR dropping to 60 dB typically [13]. From (2.19) and (2.20) it can be seen that the rejection of the first stage will also influence the +PSRR. To the first stage, a signal on V_{DD} is equivalent to a common mode signal. If the common mode rejection is poor the signal component due to the first stage will dominate at the output as seen in equation (2.19). In this case +PSRR ≈ CMRR. Note from the measurement results of both OA1 and OA2 that for the worst values of +PSRR and CMRR this is indeed the case. Note also that these cases correspond with the worst observed offsets suggesting large first stage mismatches.

5.0 CONCLUSIONS AND DISCUSSION

5.1 General design of two-stage amplifiers

Chapter 2 discussed design of two-stage op amps and a systematic design method was presented. The method aimed at meeting the primary design specifications of phase margin, slew rate, gain-bandwidth, input common mode range and output swing. Although the discussion was based on the simple capacitor compensation the techniques carry over easily to the other types of compensation. A table showing the relationships between the circuit parameters and performance areas was also given. The table allowed evaluating all the side-effects of making a circuit change aimed at improving some particular performance area.

Several points arising out of the general discussion on design should be mentioned.

1) It is important to choose the transconductance of the input pair as low as noise specifications would allow. This results in area and power savings due to a reduced compensation capacitor size as well as improved phase margin by moving the RHP zero out to higher frequency. Also the ratio of the transconductances of the mirror loads and the input pair should be made as large as possible (noise requirements set an upper limit of 1/2 on the ratio). This results in the minimum second stage current requirement of about 3 times the slew rate limit for simple capacitor compensation.
2) Both input common mode range and output swing are determined by the first stage design. The input and output range in the direction of the supply to which the current mirror load is attached is

determined by the V_{DSAT} value of these transistors. The output swing usually sets the maximum limit on this V_{DSAT} value because body effect on the input pair (assuming the body is not connected to the sources) allows the input range to easily extend to the supply. The range toward the supply to which the differential pair's current source is attached is the more difficult specification to meet. The predominant factor limiting this range is the V_{GS} of the input pair. A large aspect ratio on the current source transistor is required to minimize the contribution of its V_{DSAT} in limiting the range. Hence a small improvement in the range can be achieved only at the expense of increased area and capacitive parasitics.

3) Gain-bandwidth and slew rate requirements for a given settling time were estimated under the simplifying assumption of an integrator frequency response. For a given step size the minimum GBW and SR requirements are obtained at a particular value of V_{DSAT} for the input pair. For a 1 volt step the optimum value of V_{DSAT1} was 162 mV.

4) Power supply rejection is normally better for one supply than the other. The compensation capacitor across the second stage driver causes it to look like a diode connected transistor as frequency increases. The result is that the gain to the output from the supply to which the diode connected transistor is attached increases while the gain from the other supply decreases. Hence the PSRR of this other supply is normally superior. However, this PSRR also depends on the common mode rejection of the first stage.

If this is poor due to first stage mismatches the normally superior PSRR will also be severely degraded.

The results of measurements on the sample of five chips generally confirmed the correctness of the design methods presented. The results suggest however that the circuits should be overdesigned by a factor of about 10% for the positive input common mode range and 40% for the output swing in order to account for process tolerances. For a full discussion of the measurement results see section 4.9.

5.2 Realization in different technologies

The advantages and disadvantages of the NMOS versus PMOS input configurations were discussed. The NMOS device being in a p-well permits the removal of body effect on the input pair. Although body effect has the advantage of improving the input range it also results in degradation of power supply rejection at high frequencies due to the 'supply capacitance' effect. A disadvantage of having the input devices in a well is the higher capacitive parasitics on the sources of the input pair resulting in a higher degradation of the slew rate. PMOS inputs generally display less 1/f noise than NMOS. Also for PMOS inputs the +PSRR is normally better than the -PSRR while the opposite is true for the NMOS case.

5.3 Effects of compensation techniques on OA performance

Linear control systems analysis with s-transforms allows predicting the step response of the op amp from the open loop nondominant pole location. The optimum 0.1% settling was seen to occur for a system which was only slightly underdamped such that the overshoot was equal to the error band of 0.1%. The open-loop nondominant pole location which resulted in this corresponded with a phase margin of about 74 degrees.

With conventional compensation using only a Miller capacitor the phase margin is usually not chosen to exceed 60 degrees due to excessive power dissipation. Here the nondominant pole location is directly proportional to second stage transconductance and inversely proportional to load capacitance. Hence, high second stage current is required to counteract large load capacitance to give a desired nondominant pole location. In addition, the parallel path to the output through the compensation capacitor results in a right hand plane (RHP) zero which degrades the phase margin resulting in the need to push the nondominant pole out to higher frequency. Because of this it was shown that this type of compensation became increasingly power inefficient if the ratio of the second to first stage transconductances was not kept greater than about a factor of 6. Noise specifications set a lower limit on first stage transconductance and so in some cases it may be difficult to maintain this ratio.

The series buffer and series resistor compensation methods are more power efficient and can also result in area savings as well. Both methods allow the elimination of the RHP zero. An additional high

frequency pole and a LHP zero are introduced. Their locations are dependent on the buffer output resistance value and the series resistor value. The most power efficient choice for this value is such that the LHP zero is made to cancel the pole dependent on the load capacitor leaving only the higher frequency pole. This new nondominant pole is independent of the second stage (under the linear operation assumption) and instead is dependent on the f_T of the first stage mirror load transistors. Thus second stage bias current can then be reduced to a lower limit set by slew rate requirements. The result is a total bias current about 3 times less than the design with simple capacitor compensation. The compensation capacitor value is used to set the desired nondominant pole location relative to the unity gain frequency. It was seen that a much smaller compensation capacitor could still result in a superior phase margin. The simulation results showed a 16 degree improvement in the phase margin with a compensation capacitor less than half the size.

However, second stage nonlinear operation prevents achieving the expected optimum settling at a phase margin of 74 degrees and makes the response difficult to predict accurately. In the course of the step response the second stage driver's current level changes and hence its transconductance changes. The result is a deviation of the pole locations causing the normally cancelling pole-zero pair to split, and the nondominant pole location to change. The low second stage current results in the pole-zero pair being positioned close to the unity gain frequency and it was shown that a mismatch in this pair could strongly affect the step response. Hence the pole deviation makes the linear analysis inaccurate. Although this same effect is observed to a degree

in the simple capacitor compensation, the percentage deviation of the poles is strongest at the lower second stage bias current levels.

The nonlinearity was evident in the results of the SPICE simulations as the step response was seen to be dependent on the step size for steps up to about 2 x V_{DSAT1}. (For larger steps the first stage saturates resulting in the second stage reaching a limit in its deviation from bias conditions). Instead of resulting in the optimum settling expected according to the linear analysis, the series buffer and resistor designs with a phase margin of 74 degrees showed settling times for a rising step only slightly better than the simple capacitor compensation design with 60 degree phase margin. Still, the required compensation capacitor was about half the size and the bias current three times less. Increasing the value of the compensation capacitor so as to push the nondominant pole out to higher frequencies showed only a limited improvement in the settling time as then the splitting of the pole-zero pair became the predominant factor affecting the step response. The best results were observed when the second stage bias current was also increased from its slew rate limit. For the same size compensation capacitor and bias current as the conventional design, the series buffer and resistor designs showed an approximately 20 degree improvement in phase margin and a 30% lower settling time.

5.4 Separate stage compensation

Separate stage compensation is a different approach presented by this author. As in the previous techniques, the dominant pole is obtained by a shunt capacitance at the output of the first stage.

However, increasing the value of this capacitance through the Miller multiplication effect is here achieved by connecting the capacitor across a separate stage matched to the output stage. Another requirement is that the compensation capacitor must also be matched to the load capacitor. Because the output node is isolated from the compensation capacitor, the frequency response shows no RHP zero and the nondominant pole is independent of the second stage on the load capacitance. As in the series buffer and resistor designs, it is dependent instead on the f_T of the first stage mirror load transistors and hence can be at much higher frequency. It is then also possible to reduce the second stage bias current down to the slew rate limit. However, because of the additional stage and also because of the larger compensation capacitor, the separate stage design example has about the same power dissipation as the design with simple capacitor compensation.

Another result of the isolated output node in the separate stage design is increased attenuation at high frequencies for negative power supply noise seen at the output. Hence there is an improvement in the negative power supply rejection which is usually poor at high frequencies for a PMOS input configuration.

As in the series buffer and resistor designs, the separate stage design has a cancelling pole-zero pair (a doublet) in its frequency response. However in this case the doublet occurs at a lower frequency (approximately 0.1 w_u instead of at w_u) and its matching depends on the matching of the output and compensation stages as well as the load and compensation capacitors. Because of the lower frequency of the doublet, there is greater potential for degradation of the settling

time. It was shown that the pole and zero need to be matched within about 5% to prevent degradation for 0.1% settling. How this requirement translates into process tolerances remains to be shown. However, for the small sample of five chips the settling times indicated quite a variation in the mismatch which suggests that the required degree of matching may not be possible. The results also indicated that the total output loading should be accounted for in the compensation capacitor to prevent additional pole/zero mismatch.

As opposed to the series buffer and resistor case, the doublet in the separate stage case does not split when the second stage current changes during the step response. In addition, although the current change also results in deviation of the high frequency pole, this has little effect on the response because first stage phase shift becomes the dominant factor in setting the 'equivalent' nondominant pole location. The result is that even if the second stage has the low bias current, its nonlinearity has less effect on the step response than in the series resistor and buffer cases.

Measurement results confirmed an approximately 20 degree improvement in phase margin resulting in the step response having no ringing and a 20% reduction in settling time when matching was sufficient. Also, an approximately 20 dB improvement in the negative power supply rejection was observed for frequencies above 100 kHz.

5.5 Concluding remarks and future research

Compared to the separate stage design the series resistor and buffer designs showed better area efficiency for the same power

dissipation as well as improved settling by about 10%. However, some of this advantage would be negated if meeting noise specifications requires the series buffer and resistor designs to have a large first stage transconductance as in the separate stage design. Of the series buffer and resistor compensation methods, the latter would be preferred since it does not reduce the output swing and results in less power dissipation. An area for future research in series resistor compensation would be to investigate circuitry aimed at having the zero of the doublet track the pole in the course of the step response. Hence the effect of the second stage nonlinearity at low current levels would be reduced resulting in a better step response and better power efficiency. It is felt that the class AB circuit configuration of figure 2.30 [13] should display this type of behaviour. The devices of the output stage operate in a push-pull arrangement resulting in a pole location dependent on the sum of the transconductances of the two devices. During the course of the step response one transconductance increases while the other decreases and hence the overall pole deviation should be less. The class AB nature of the circuit has the added advantage of improving the slew rate.

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APPENDIX 1: Estimation of SR and GBW for a given t_S

Using the simple model of figure A1.1, the step response of the OA with 100% feedback can be shown [12, p. 279] to be as given in figure A1.2. From [12, eqn. 9.8] we have:

$$t_S = \frac{V_S}{SR} - \tau + \left(\tau \ln\left[\frac{SR\ \tau}{\epsilon\ V_S}\right]\right) \qquad (A1.1)$$

where V_S = step size and ϵ = error factor (i.e. ϵ = .001 for 0.1% settling) the first bracketed term of (A1.1) represents the time spent slewing. SR and GBW for the OA of figure 2.1 can be shown [21] to be related:

$$\begin{aligned} SR &= I_5/Cc = (I_5/g_{m1})GBW = 2(I_1/g_{m1})GBW \\ &= (V_{GS1} - V_{t1})GBW \\ &= V_{DSAT1}/\tau \end{aligned} \qquad (A1.2)$$

For minimizing offset V_{DSAT1} should be chosen less than about 200 mV (see section 2.2.9). Substituting (A1.2) into (A1.1) and assuming 0.1% settling gives:

$$t_S = [(V_S/V_{DSAT1})-1]\tau + [7-\ln(V_S/V_{DSAT1})]\tau \qquad (A1.3)$$

$$= [6+(V_S/V_{DSAT1})-\ln(V_S/V_{DSAT1})]\ (1/GBW) \qquad (A1.4)$$

Hence

$$GBW[MHz] = \frac{1}{2\pi}\frac{[6+(V_S/V_{DSAT1})-\ln(V_S/V_{DSAT1})]}{t_S[\mu s]} \qquad (A1.5)$$

and from (A1.2)

$$SR[V/\mu s] = 2\pi\ GBW[MHz]\ V_{DSAT1} \qquad (A1.6)$$

These equations are used to generate the curves of figure 2.8. The curves give the SR and GBW requirements for 0.1% settling of a 1 V step for different values of V_{DSAT1}.

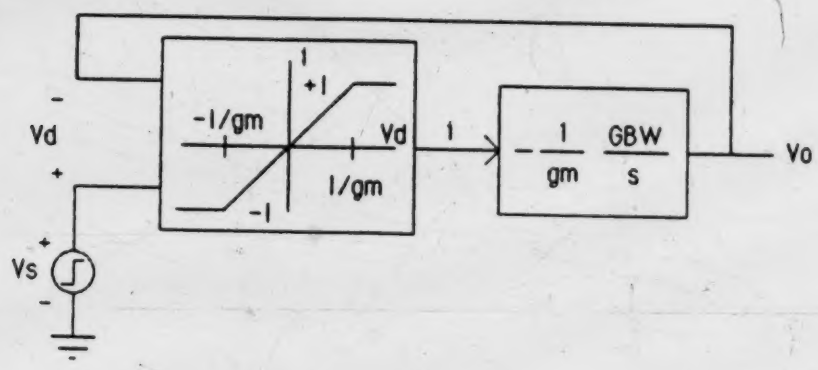

Figure A1.1 Simplified model of the OA in the non-inverting unity gain configuration.

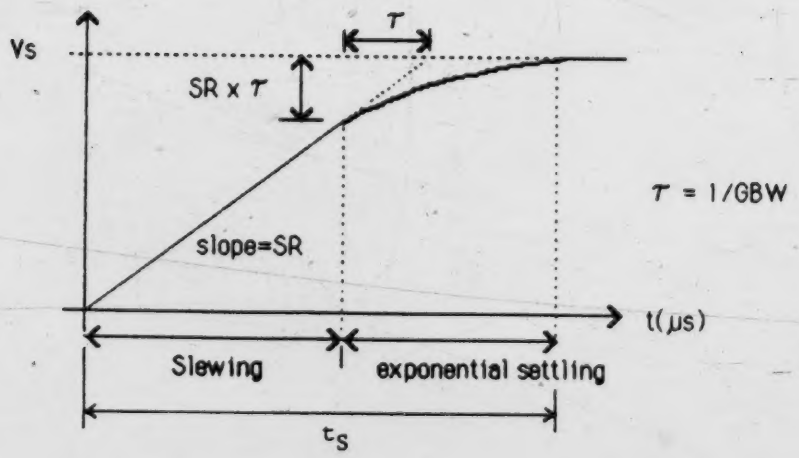

Figure A1.2 Step response for the circuit of fig A1.1

Note that at a larger V_{DSAT1}, the required GBW is less but the required SR is more. The reason is that the portion of the settling time in which slewing occurs becomes less. From (A1.5) and (A1.6) the product GBW x SR can be shown to be a minimum for $V_S/V_{DSAT1} \sim 6.18$ (V_{DSAT1} = 162 mV when V_S = 1 V) which corresponds to equal time spent in slewing as in exponential settling. Note from figure 2.8 that for this case GBW[MHz] ~ SR[V/μs].

APPENDIX 2: ICMR and OS Requirements

The following refers to the PMOS input configuration of figure 2.1. For -ICMR, M1 and M2 leave pinchoff when the gate voltage drops $|V_{t1}|$ below the drain voltage which is set by the current mirror load. Hence the requirement:

$$(Vi_{min} - V_{SS}) - V_{GS3} \geq |V_{t1}|$$

$$V_{GS3} \leq (Vi_{min} - V_{SS}) - |V_{t1}| \qquad (A2.1)$$

$$V_{DSAT3} \leq (Vi_{min} - V_{SS}) - |V_{t1}| - |V_{t3}|$$

Here V_t is calculated using [1]:

$$V_t = V_{to} + \gamma \left(\sqrt{2\phi_F + |V_{SB}|} - \sqrt{2\phi_F} \right) \qquad (A2.2)$$

The -OS sets the requirement:

$$V_{DSAT6} \leq Vo_{(min)} - V_{SS}$$

and since the gate voltages of M3 and M6 are the same we have $V_{DSAT3} = V_{DSAT6}$ and

$$V_{DSAT3} \leq Vo_{(min)} - V_{SS} \qquad (A2.3)$$

(A2.1) and (A2.3) set the upper limit on V_{DSAT3} and since the MOSFET current is given by:

$$I = \frac{K'}{2} \frac{W}{L} (V_{DSAT})^2 \qquad (A2.4)$$

we have

$$(W/L)_3 \geq \frac{I_5}{K_n' (V_{DSAT3(max)})^2} \qquad (A2.5)$$

For +ICMR, M5 will leave pinchoff when its V_{DS} becomes less than V_{DSAT5}. Hence the requirement to prevent this is

$$V_{DSAT5} \leq (V_{DD} - Vi_{max}) - |V_{GS}| \qquad (A2.6)$$

Using (A2.4) this gives

$$V_{DSAT5} \leq (V_{DD} - Vi_{max}) - \left[\sqrt{\frac{I_5}{K_p'(W/L)_1}} + |V_{t1}|\right] \qquad (A2.7)$$

For +OS, preventing M7 from leaving pinchoff requires

$$V_{DSAT5} \leq V_{DD} - Vo_{max} \qquad (A2.8)$$

and since M5 and M7 have a common gate this gives

$$V_{DSAT5} \leq V_{DD} - Vo_{max} \qquad (A2.9)$$

From (A2.7) and (A2.9) $V_{DSAT5(max)}$ is found. Then from (A2.4) we have:

$$(W/L)_5 \geq \frac{2\ I_5}{K_p'(V_{DSAT5max})^2}$$

Appendix 3: Spice file for design example

```
ptwo-stage OA,C1=20pf
.OPTIONS OPTS NUMDGT=6 RELTOL=0.000001 LIMPTS=700
.WIDTH IN=80 OUT=80
*
*VIN+ 8 0 PWL(0 0 10N 0 20N .1 3U)
VIN+ 8 0 DC 0 AC 0
VIN- 9 0 DC 0 AC 1.0
VDD 1 0 DC 5
VSS 0 2 DC 5
IBIAS 3 2 DC 8.6UA
*
M1 5 9 4 1 PMOS5 W=78U L=10U AD=936P AS=936P PD=102U PS=102U
M2 6 8 4 1 PMOS5 W=78U L=10U AD=936P AS=936P PD=102U PS=102U
M3 5 5 2 2 NMOS5 W=10U L=10U AD=120P AS=120P PD=34U PS=34U
M4 6 5 2 2 NMOS5 W=10U L=10U AD=120P AS=120P PD=34U PS=34U
M5 4 3 1 1 PMOS5 W=64U L=10U AD=768P AS=768P PD=88U PS=88U
M6 7 6 2 2 NMOS5 W=240U L=10U AD=2880P AS=2880P PD=264U PS=264U
M7 7 3 1 1 PMOS5 W=768U L=10U AD=9216P AS=9216P PD=792U PS=792U
M8 3 3 1 1 PMOS5 W=64U L=10U AD=768P AS=768P PD=88U PS=88U
* compensation
CCOMP 7 6 4.4PF
* output load
CLOAD 7 0 20PF
*
* nmos, 5 micron, w mob deg, w vel satn
*
.MODEL NMOS5 NMOS (LEVEL=2
+VTO=0.9 PB=0.7
*+IS=1E-14
+JS=1.37E-5
+TOX=8.5E-8 NSUB=9.92E15 XJ=1E-6
+LD=7.0E-7 UO=750
+UCRIT=6.44E4 UEXP=0.139 VMAX=4.92E5
+CSGO=2.84E-10 CGDO=2.84E-10 CGBO=2.0E-10
*+CBD=4E-14 CBS=4E-14
+CJ=3.44E-4 MJ=0.5 CJSW=1.09E-9 MJSW=0.5
+XQC=0.4
*
* pmos, 5 micron, w mob deg, w vel satn
*
.MODEL PMOS5 PMOS (LEVEL=2
+VTO=-0.9 PB=0.7
*+IS=1E-14
+JS=4.19E-10
+TOX=8.5E-8 NSUB=1.98E15 XJ=9E-7
+LD=6E-7 UO=240
+UCRIT=1.23E4 UEXP=0.022 VMAX=7.33E4
+CSGO=2.44E-10 CGDO=2.44E-10 CGBO=2.00E-10
*+CBD=1.8E-14 CBS=1.8E-14
+CJ=1.54E-4 MJ=0.5 CJSW=4.37E-10 MJSW=0.5
+XQC=0.4
```

```
*
*measure freq response
.AC DEC 10 10HZ 10GHZ
.PRINT AC VDB(7) VP(7)
*measure step response
*.TRAN 0.005U 3U
*.PLOT TRAN V(7) V(8) (.0997,.1001)
*.OP
.END
```